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WAVETEK
SAN DIEGO

9045 BALBOA AVENUE, SAN DIEGO, CALIFORNIA

Serial No. _____

INSTRUCTION MANUAL

MODELS 158 AND 159 PROGRAMMABLE WAVEFORM GENERATORS

(Plus Option 159-005 Data)

NOTICE

Option 159-005, IEEE 488 Interface, data is included in the back of this manual.

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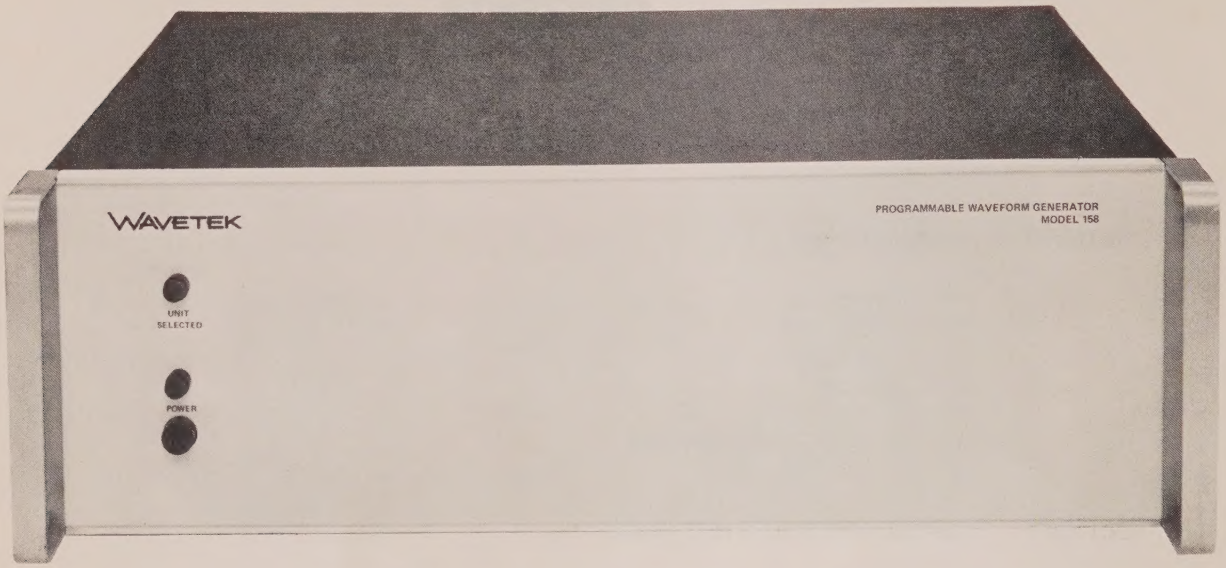
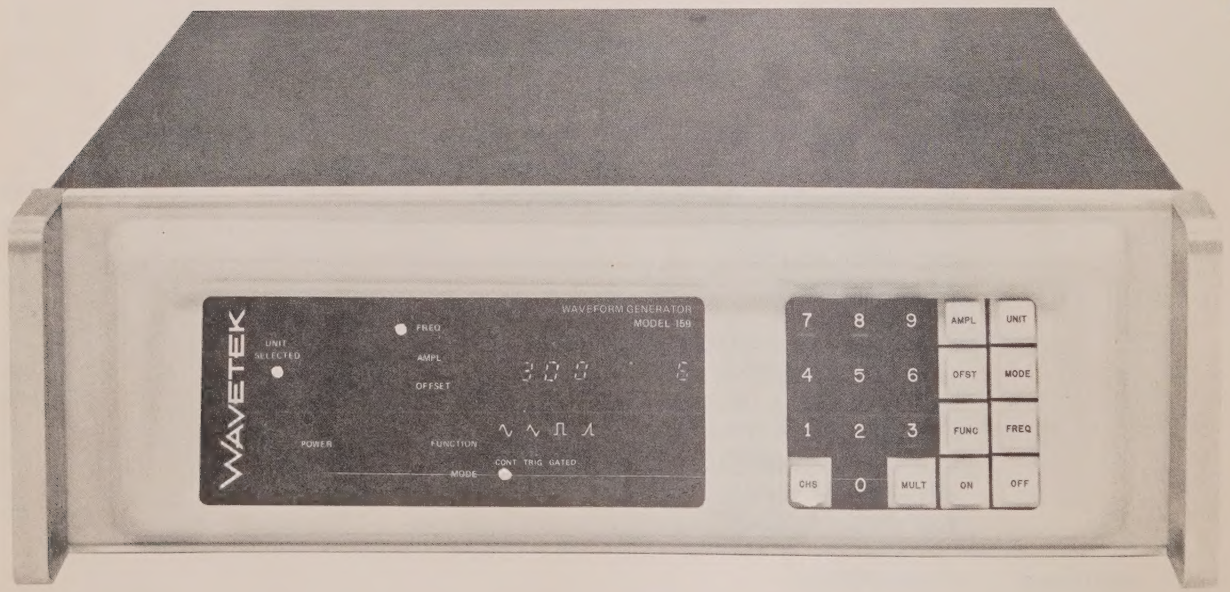


Wavetek Model 158 Programmable Waveform Generator



Wavetek Model 159 Programmable Waveform Generator

Figure i – Model 158 and 159 Programmable Waveform Generators

SECTION 1
INTRODUCTION

1.1 MODEL 158

The Wavetek Model 158 Waveform Generator is a remote-control only Model 159 generator (without front panel controls and indicators). All information on the Model 159 generator also pertains to the Model 158 generator except local operation.

1.2 MODEL 159

The Wavetek Model 159 Waveform Generator is digitally controlled locally with front panel, keyboard pushbuttons, and remotely with a selection of 21 ASCII (7-level) "typing" characters (with appropriate external interface). The effect of each control is digitally displayed on the front panel with red LED (light emitting diode) indicators. Numeric readout of frequency, offset and amplitude is in 3-digit scientific notation.

Sine, triangle, square, and ramp waveforms of frequencies from 1 Hz to 3 MHz and amplitudes from 10 mV p-p to 10V p-p can be generated. Waveform generation can be continuous, triggered for just one cycle at a time, or gated for as many cycles or for as long as desired. Waveform center reference levels can be offset positive or negative from 10 mV to 5V and waveform phase, or polarity, can be inverted (180 degrees).

Along with the main 50 ohm output at the rear panel, which is the controlled waveform signal output, the generator delivers a square wave of the selected frequency for a synchronizing pulse output.

Analog inputs are received at the rear panel for a triggering input for triggered and gated operations, and a voltage controlled generator (VCG) input for frequency proportional to input dc levels. The 50Ω OUT signal can be swept in a 1000:1 frequency ratio, frequency modulated or dc programmed by the VCG input. The trigger and gate modes can be used for pulse output, one cycle output or tone bursts.

Up to nine generators can be connected in parallel with one another as a multiple unit group. Each generator is internally configured with its own address, or unit select code, from 1 to 9. For example, an installation may have one master display and keyboard panel, which is used to address and command the slave generators. The status of the addressed generator would be displayed.

1.3 INTERFACE

The generator accepts TTL ground true 7-bit ASCII "typing" characters serially; the 7 bits of each character are accepted in parallel. A clock line in parallel with the data bits is used to clock in the data characters. Computer control is accepted as is keyboard control from another generator in multiple unit groups. With computer control, the generator keyboard control panel can be locked out, or disabled, to prevent control competition.

1.4 OPTIONS

Several interface options are available for the Model 158 and 159 generators. They include input isolation, RS232 and IEEE 488 compatible data converters.

1.5 ACCESSORIES

Accessories for the generators include interfaces for several mini-computers.

1.6 PHYSICAL DESCRIPTION

The mechanical characteristics of the Models 158 and 159 are given in Paragraph 1.7.8. The standard models come equipped with a 10 foot, 3 wire detachable power cord and rack mount adapters. Interface cabling requires Molex brand connectors (see Paragraph 2.2.3); one is furnished.

1.7 SPECIFICATIONS

1.7.1 Versatility

Waveforms

Sine ∿ , triangle △ , square ⎍ , ramp ◿ (50% duty cycle), and auxiliary TTL sync pulse. All selectable waveforms may be inverted.

Frequency Range

Sine, triangle, and square from 1 Hz to 3 MHz in 7 ranges with 3-digit resolution.

10^0	1 Hz to 9.99 Hz
10^1	10 Hz to 99.9 Hz
10^2	100 Hz to 999 Hz
10^3	1 kHz to 9.99 kHz
10^4	10 kHz to 99.9 kHz
10^5	100 kHz to 999 kHz
10^6	1 MHz to 3 MHz

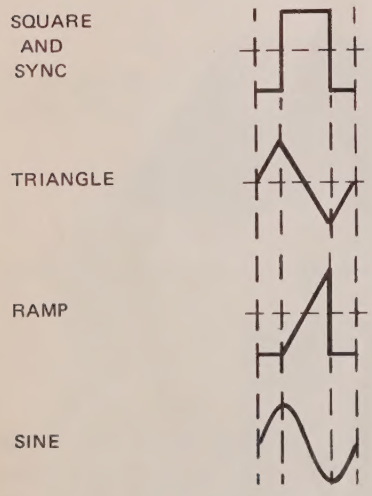
Ramp from 1 Hz to 1 MHz in 6 ranges ($10^0 \longrightarrow 10^5$).

NOTE

Generator is usable from 0.01 Hz with derated accuracies.

Main Output

Three digits of amplitude from 10 mV to 10V p-p into 50Ω (20V p-p into an open circuit) in 3 ranges (10^0, 10^{-1}, 10^{-2}).



NORMAL PHASE RELATIONSHIPS

DC Offset

Three digits of dc offset to ±5V into 50Ω. DC offset plus waveform peak value may not exceed 10V peak into open circuit or 5V peak into 50Ω.

Sync Output

A TTL compatible 0 to 2.5V square wave output, which provides 50 mA sinking current to sync up to 30 TTL loads.

Data Entry

Front panel keyboard/display and remote programming (Model 159).
Remote programming only (Model 158).

1.7.2 Operational Modes

Continuous, triggered, and gated operation provided. In triggered mode, one cycle of selected signal output for each input trigger signal. In gated mode, signal output at selected frequency for duration of the input gate plus completion of the last cycle. Model 159 has front panel manual trigger.

Trigger/Gate Signal

Minimum	+2V
Maximum	50V
Input Impedance	1 kΩ

1.7.3 Analog Modulation Control

Frequency may be externally controlled by analog voltage (VCG) providing dc programming for FSK or wide band ac modulation. Input impedance is 5 kΩ.

VCG Control Signal

Approximately 2.5V	1000:1 frequency change
Approximately 7.5V	3000:1 frequency change (300% overrange in first 6 ranges)

VCG Small Signal Bandwidth

100 kHz

VCG Slew Rate

4% of range per μs

1.7.4 Accuracy

Horizontal Precision (Frequency Accuracy)

10 Hz to 100 kHz	±1% of program value ±1 digit
100 kHz to 1 MHz	±2% of program value ±1 digit
1 MHz to 3 MHz	±4% of program value ±1 digit

Vertical Precision (Amplitude Accuracy)

NOTE

Vertical precision stated is for 10^0 amplitude multiplier. For 10^{-1} and 10^{-2}, add 1% per step.

Vertical Precision (Amplitude Accuracy) (Continued)

Sine and Square Waveforms:
10 Hz to 100 kHz . . . ±2% of program value ±1 digit
100 kHz to 1 MHz . . . ±5% of program value ±1 digit

Triangle and Ramp Waveforms:
10 Hz to 10 kHz . . . . ±2% of program value ±1 digit

DC Offset

±2% of program value ±1 digit

Sine Wave Frequency Response

Amplitude change with frequency less than:
0.1 dB to 100 kHz
0.5 dB to 1 MHz
1.0 dB to 3 MHz

Stability

Short term . . . . . ±0.05% for 10 minutes
Long term . . . . . ±0.25% for 24 hours

1.7.5 Purity

Sine Wave Distortion

Total harmonic distortion less than:
0.5% to 30 kHz . . . . . ranges 10^0 thru 10^3
1.0% to 300 kHz . . . . . ranges 10^0 thru 10^4

All harmonics:
34 dB down to 1 MHz

Time Symmetry

1% to 100 kHz

Amplitude Symmetry

All waveforms to 100 kHz are symmetrical about ground within 1% of maximum p-p amplitude.

Triangle Linearity

Greater than 99% to 100 kHz

Square Wave Rise and Fall Time

Less than 50 ns

Total Aberrations

Less than 5% of program value ±20 mV

1.7.6 Programming

Programming Transition Time

Unit accepts bytes at a 1 MHz rate. The output will become stable within 100 μs unless the range digit is changed; then output will be stable within 1 ms.

Isolation

Signal ground and program ground are common in the standard 158/159. Optical isolation is available.

Logic Level Requirements

State	Requirements
Low (Logic "1")	0V to 0.4V sinking 25 mA maximum
High (Logic "0")	2.4V or open

NOTE

1. *Open input is 3.0V.*
2. *Input is terminated by 220Ω to +5V and 330Ω to ground.*
3. *Recommended driver: SN 7438.*

Input Control Lines and Connector Layout

Mating Connector: Molex 03-09-2151 with 02-09-2118 pins

J9 Pin No.	Designation	
13	XD0	Least significant bit
11	XD1	
8	XD2	
10	XD3	Input data lines
9	XD4	
12	XD5	
14	XD6	Most significant bit
15	XCLK	Clock control
7	Common	
3	Keyboard Enable	
1	Keyboard Enable Return	

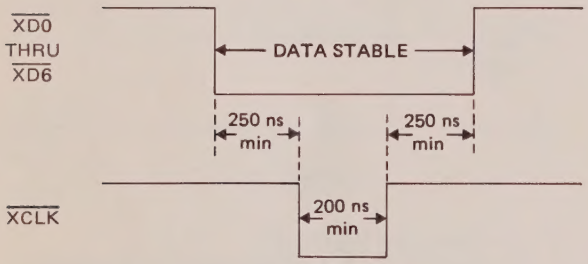
Keyboard to ASCII Conversion Table

Keyboard	ASCII
AMPL	A
UNIT	G
OFST	D
MODE	B
FUNC	C
FREQ	F

Keyboard	ASCII
MULT	(Space) or E
ON	H
OFF	I
0 thru 9	0 thru 9
CHS	– (Minus)

Timing

Direct (No Isolation)



1.7.7 Environmental

Specifications apply for 25°C ±5°C. For operation from 0°C to +55°C, derate all specifications by a factor of 2. Unit may be stored from −40°C to +75°C without damage.

1.7.8 Mechanical

May be used on the bench or in a 19 inch rack. Rack adapter hardware and program mating connectors included.

Dimensions

17¼ in./43.8 cm wide, 5¼ in./13.3 cm high, 17 in./43.2 cm deep.

Weight

15 lb/6.8 kg net, 23 lb/10.4 kg shipping.

Power

90 to 110V, 105 to 125V, 180 to 220V, or 210 to 250V; 50 to 400 Hz. Less than 45 watts.

NOTE

Specifications apply for settings from 1.00 to 9.99

SECTION 2
INSTALLATION AND INTERFACE

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

The standard generator is a bench-top instrument with a collapsible tilt-bail to elevate its front end for convenient viewing.

The generator can also be rack mounted by attaching the rack mount adapters to the sides.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 105 - 125 Vac line supply and with a ¾ amp slow-blow fuse.

Conversion for 90 to 110V, 180 to 220V, or 210 to 250V operation requires resetting two switches on the inside of the rear panel. To reset the switches, remove the top cover for access. Set the two switches and select the fuse for the ac line voltage according to the following table.

AC Line Voltage	Switch A	Switch B	Fuse (SB)
90 - 110	115	LO	3/4 amp
105 - 125	115	HI	3/4 amp
180 - 220	230	LO	3/8 amp
210 - 250	230	HI	3/8 amp

Connect the ac line cord to the mating connector at the rear of the unit.

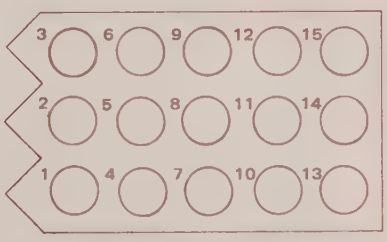
2.2.2 Signal Connections

Use 50Ω shielded cables equipped with female BNC connectors to distribute 50Ω OUT, SYNC OUT, TRIG IN and VCG IN signals when connecting this instrument to associated equipment.

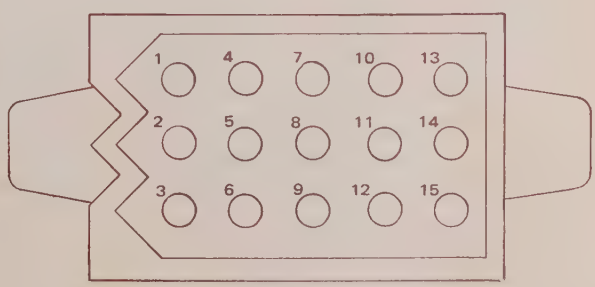
2.2.3 Control Connections

The remote (ASCII DATA IN/OUT) rear panel connection, harness wire colors, pin connections and signal names are given in Tables 2-1 and 2-2.

The remote connector is a Molex 03-09-1151 which mates with a Molex 03-09-2151 connector housing with up to 15 Molex 02-09-2118 pin contacts. Pin contacts are prepared using a Molex Model A6973 Crimping Tool to connect No. 18 or No. 22 wire (strip back 1/10 to 1/8 inch).



MOLEX 03-09-1151



MOLEX 03-09-2151

Figure 2-1. Connectors (Socket/Pin Sides)

Table 2-1. ASCII DATA IN/OUT AND HARNESS CONNECTORS

Pin	Connector: ASCII Data In/Out (Rear Panel) Wire Color	ASCII Data In/Out (Rear Panel) Signal	Keyboard Harness Wire Color	Keyboard Harness Signal	Display Harness Wire Color	Display Harness Signal
1	1	PCOM				
2	2					
3	3	KINH	2	KINH		
4			1	+5V	7	+5V
5	5					
6	6	BUSY				
7	7	COM	91	COM	0	COM
8	8	XD2	8	KD2	1	DCLK
9	9	XD4	5	KD4		
10	90	XD3	3	KD3	2	DD0
11	91	XD1	7	KD1	4	DD2
12	92	XD5	4	KD5		
13	93	XD0	90	KD0	6	DSYNC
14	94	XD6	6	KD6	3	DD3
15	95	XCLK	9	KCLK	5	DD1

Code	Color	Code	Color
0	Black	8	Gray
1	Brown	9	White
2	Red	90	White with black tracer
3	Orange	91	White with brown tracer
4	Yellow	92	White with red tracer
5	Green	93	White with orange tracer
6	Blue	94	White with yellow tracer
7	Violet	95	White with green tracer

PCOM: Input Program Common
KINH: Keyboard Inhibit (When connected to pin 7)
COM: Signal Common
X: External
D: Data
0 - 6: Bits 0 thru 6
CLK: Clock
K: Keyboard
D: Display

Table 2-2. KEY, ASCII, HEXADECIMAL, AND BINARY CODES FOR PROGRAMMING FUNCTIONS

Control and Data Names	Model 159 Key	ASCII Character and TTY Keyboard	Hexa-Decimal Code	Binary (and ASCII Bus) Bit 7 XD6	Bit 6 XD5	Bit 5 XD4	Bit 4 XD3	Bit 3 XD2	Bit 2 XD1	Bit 1 XD0
Range (X 10 mult)*		(Space)	20	0	1	0	0	0	0	0
Invert phase/offset	CHS	–	2D	0	1	0	1	1	0	1
0	0	0	30	0	1	1	0	0	0	0
1	1	1	31	0	1	1	0	0	0	1
2	2	2	32	0	1	1	0	0	1	0
3	3	3	33	0	1	1	0	0	1	1
4	4	4	34	0	1	1	0	1	0	0
5	5	5	35	0	1	1	0	1	0	1
6	6	6	36	0	1	1	0	1	1	0
7	7	7	37	0	1	1	0	1	1	1
8	8	8	38	0	1	1	1	0	0	0
9	9	9	39	0	1	1	1	0	0	1
P-P amplitude	AMPL	A	41	1	0	0	0	0	0	1
Operating mode	MODE	B	42	1	0	0	0	0	1	0
Function (waveform)	FUNC	C	43	1	0	0	0	0	1	1
Reference offset	OFST	D	44	1	0	0	0	1	0	0
Range (X 10 mult)*	MULT	E	45	1	0	0	0	1	0	1
Frequency	FREQ	F	46	1	0	0	0	1	1	0
Unit select address	UNIT	G	47	1	0	0	0	1	1	1
Output on	ON	H	48	1	0	0	1	0	0	0
Output off	OFF	I	49	1	0	0	1	0	0	1

1 = True = Low
0 = False = High

*See the second entry of this control name.

SECTION 3
OPERATION

3.1 INITIAL CHECKOUT

To ensure that the generator is operating properly, make the power and interface connections (Section 2), and operate the generator, function-by-function, as described in the following paragraphs.

3.2 CONTROLS, INDICATORS AND PROGRAMMING

Programming instructions and considerations for the Model 158 and 159 generators are the same, except for keyboard enable control that only applies to the Model 159 generator.

The Model 159 has a 20-pushbutton front panel keyboard to provide the same control as the Model 159 or 158 20 remotely programmed ASCII character bytes.

The 20 generator controls and their various code conversions are listed in Table 2-2. The Model 159 front panel controls and indicators are shown in Figure 3-1.

3.2.1 Power

Power is turned on and off with the PWR pushbutton. When the power is turned on, the generator is automatically addressed and is ready to accept commands. If a different generator is to be addressed, use the UNIT control (refer to Paragraph 3.2.4). Also, when the power comes on, the output is automatically disabled to allow the loading of a program; line transients on the output are also avoided. The generator must get an ON command to provide an output (refer to Paragraph 3.2.5).

3.2.2 Indicators

The Model 159 indicators turn on to indicate the various functions, modes, quantities, sign, and address programmed; the numerals displayed are significant as frequency, amplitude or offset, but only one category at any one time. The 3-digit number is always a 1-digit whole number and a 2-digit decimal. The three digits are displayed in order of entry, shifting right-to-left as shown in Table 3-1. The single digit is a power of ten. (Only the last three entered significant

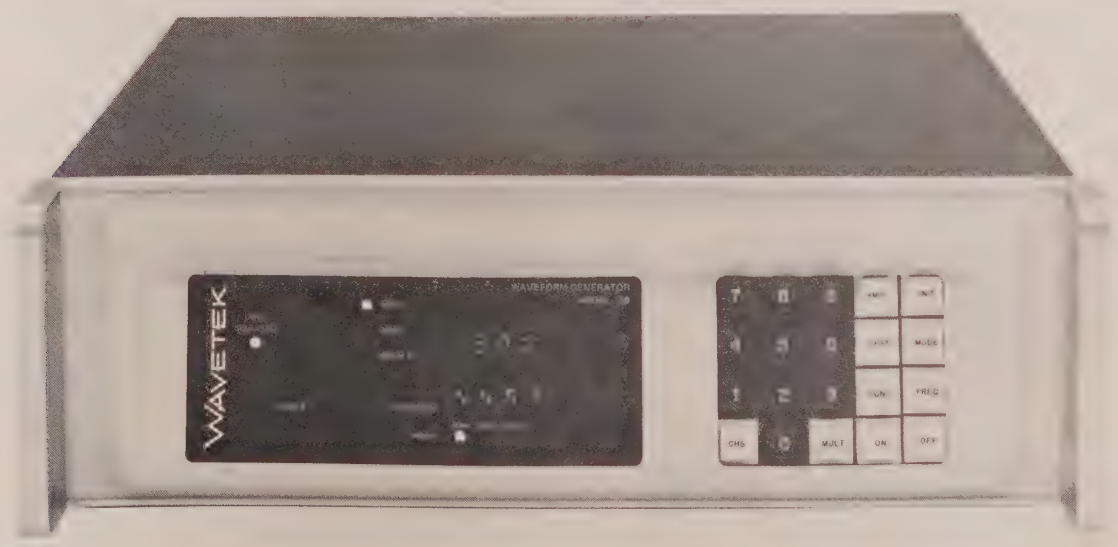


Figure 3-1. Model 159 Waveform Generator

digits and the last entered digit for the power of ten are stored. Any previously entered digits of the significant digits or the power of ten are shifted out of memory.)

3.2.3 Programming

Programming is mostly a matter of prefixing, by sequence, the numerical values and numeric codes with their intended use. For example, programming a continuous 5.79 kHz sine wave on Unit No. 1 is given in Table 3-1.

Table 3-1. EXAMPLE OF PROGRAMMING

Sequence	Wavetek Keyboard	Remote ASCII	Lighted Display
1	UNIT	G	–––
2	1	1	SELECT
3	MODE	B	–––
4	0	0	CONT
5	FUNC	C	–––
6	0	0	∿
7	FREQ	F	–––
8	5	5	0.05
9	7	7	0.57
10	9	9	5.79
11	MULT	E	–––
12	3	3	3 (power of ten)

Table 3-2. KEYBOARD TO ASCII CONVERSION TABLE

Keyboard	ASCII	Keyboard	ASCII
AMPL	A	MULT	(Space) or E
UNIT	G	ON	H
OFST	D	OFF	I
MODE	B	0 thru 9	0 thru 9
FUNC	C	CHS	– (Minus)
FREQ	F		

Generally, alpha characters (A thru I) are subsection addresses and are usually followed by one or more numeric digits representing a value or control selection.

NOTE

Any character may be separated by spaces, periods or other characters not defined here. Spaces may be inserted between alpha control characters and numeric fields; however, a space will move from a value field to the exponent field where scientific notation is used after at least one numeric digit has been received. (See Paragraphs 3.2.8 and 3.2.9.)

The generators are designed to accept a scientific notation input format. System programmers using FORTRAN will find that the result of the format statement

20 FORMAT (1 HF, 1PE13.3)

will control the frequency without additional processing.

The following paragraphs describe the program elements and give their ASCII codes. The Model 159 front panel keys correspond one-for-one with the ASCII codes; if there is any doubt as to correspondence, refer to Table 3-2.

3.2.4 Unit Selected Address

After the unit prefix (G), program one digit to select the unit. The unit addressed in a multiple-unit group responds to subsequent commands; other units do not. Generators are given the address of 1 at the factory unless specified otherwise at the time of purchase. Address changes are easily made in the field. Subsequent instructions will be accepted by the last unit addressed.

3.2.5 Output On/Off

The generator output is enabled by programming H and inhibited by programming I. H and I connect and disconnect the generator output to the external BNC connector.

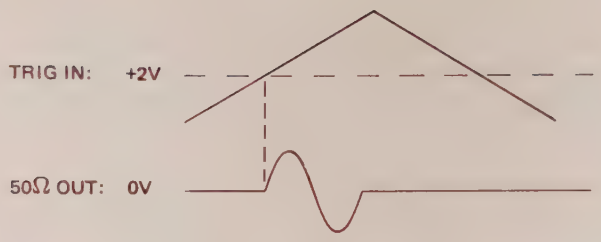
3.2.6 Operating Mode

Operating Mode	ASCII Character
Continuous	0
Triggered	1
Gated	2

After the mode prefix (B), program one digit to select the desired mode.

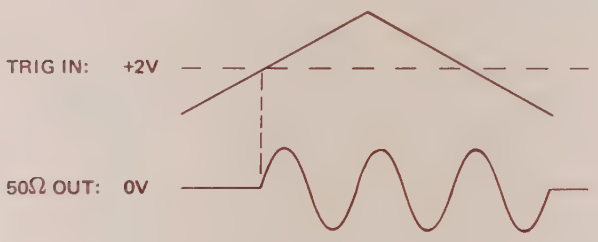
The generator output can be made to run continuously, triggered for just one cycle of waveform at a time, or gated for as many cycles or for as long as desired.

The triggered and gated modes require an external trigger level input at rear panel connector TRIG IN of at least +2V, not to exceed +50V; inputs below +2V are not to exceed –50V. In the triggered mode, one cycle of waveform is generated whenever the input at TRIG IN increases positively thru +2V.



In triggered mode, the generator may be "manually" triggered by pressing the "1" key or programming an ASCII 1.

In the gated mode, waveforms are generated for as long as the input at TRIG IN stays above +2V. When the input at TRIG IN falls below +2V, the last cycle of waveform is completed and the waveform stops.



3.2.7 Function (Waveform)

Waveform	ASCII Character
Sine	0
Triangle	1
Square	2
Ramp	3

After the function prefix (C), program one digit to select the desired waveform. Waveforms can be inverted during amplitude selection.

3.2.8 Frequency and Multiplier

After the frequency prefix (F), program a 3-digit number (1.00 to 9.99) for the three most significant digits; after the multiplier prefix (E or space), program the power of 10 (0 thru 6).

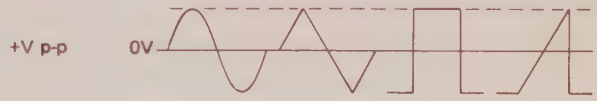
3.2.9 Amplitude and Multiplier

After the amplitude prefix (A), program (–) if waveform inversion is desired; then, program a 3-digit number (0.00 to 9.99) for the three most significant digits. After the multiplier prefix (E or space), program the power of 10 (0, 1 or 2). Powers 1 and 2 are automatically accepted as –1 and –2. Amplitude is volts peak-to-peak into a 50Ω load.

NOTE

DC offset plus waveform peak value may not exceed 10V peak into an open circuit or 5V peak into 50Ω.

All waveforms including ramp have a center reference level. Notice the inversion caused by programming –V p-p. Normal waveforms start in the positive direction regardless of their offset. Inverted waveforms start in the negative direction regardless of their offset.



3.2.10 Signal Reference Offset

After the offset prefix (D), program (–) if negative offset is desired; then, program a 3-digit number (0.00 to 5.00) for the offset significant digits. The offset multiplier, or range, is the amplitude program multiplier. For example, if A150E1 and D350 are programmed, the waveform will be +0.15V p-p with an offset of +0.35V.

Offset control allows the generator output reference level to be offset, or displaced positive or negative to 5V. All waveforms including ramp have a center reference level from which the offset is made.

NOTE

DC offset plus waveform peak value may not exceed 10V peak into an open circuit or 5V peak into 50Ω.

3.3 OPERATING PROCEDURE

No preparation for operation is required beyond the completion of the initial installation checks. Allow the generator and associated equipment to warm up for specified generator accuracies. Refer to the control descriptions given in Paragraph 3.2 for actual keyboard or remote commands.

3.3.1 Operating as a Basic Waveform Generator

1. Terminate the 50Ω OUT connector with a 50Ω ±0.1% termination.

2. Select the desired waveform and continuous mode.

3. Select the desired frequency, output amplitude and offset.

NOTE

DC offset plus waveform peak value may not exceed 10V peak into an open circuit or 5V peak into 50Ω. Specifications apply for frequency and amplitude programs from 1.00 to 9.99.

3.3.2 Operating as a Voltage Controlled Generator

VCG operation is the same as the basic waveform operation plus the connection of a VCG voltage source to the VCG IN connector. Input impedance is 5 kΩ.

The VCG input can be used to externally control the frequency of the 50Ω OUT signal. A positive voltage applied to the VCG IN connector will increase the generator frequency, and a negative voltage will decrease the frequency. A 2.5V excursion can vary the frequency by a factor of 1000, and a 7.5V excursion will allow 300% overranging, as shown in the following table.

Range	1:3000 (300% Overrange)
10^0	0.01 Hz to 30 Hz
10^1	0.1 Hz to 300 Hz
10^2	1 Hz to 3 kHz
10^3	10 Hz to 30 kHz
10^4	100 Hz to 300 kHz
10^5	1 kHz to 3 MHz

The nomograph of Figure 3-2 shows the characteristics of the VCG circuit. Column A gives the 3-digit program setting; column B, the VCG IN voltage; and column C, the factor representing the resultant frequency of the generator (multiply by range for actual frequency). As an example of nomograph use, suppose you want to operate at a basic frequency of 350 kHz and vary the frequency by VCG voltage from 100 kHz to 2 MHz. Mark the 3.50 3-digit program setting in column A on the nomograph. Draw a line to each of the frequency limits in column C, 20.0 and 1.00. In the VCG IN Voltage column, the voltage range defined by these two lines is the VCG IN operating range. In the example, the VCG voltage range is from −0.60 to 4.15 volts.

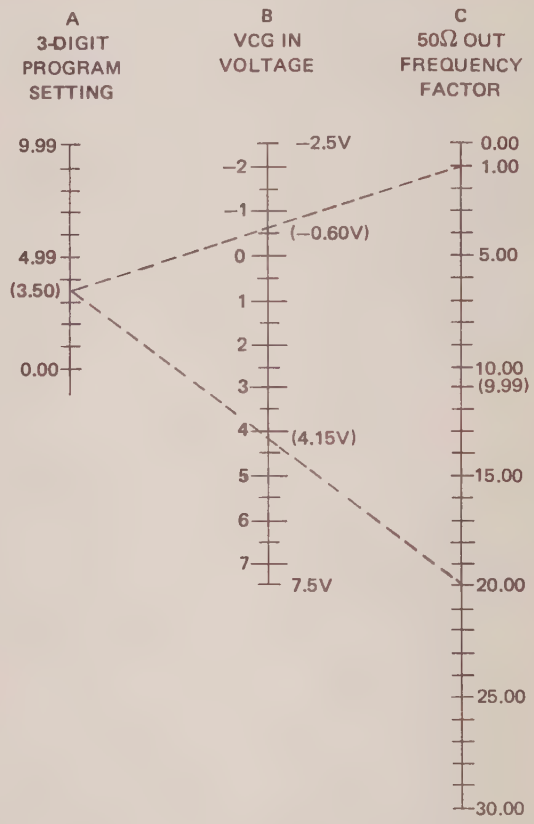


Figure 3-2. VCG Nomograph

3.3.3 Operating as a Triggered/Gated Waveform Generator

Trigger/gate operation is the same as the basic waveform operation plus the connection of a trigger source to the TRIG IN connector and the selection of TRIG or GATED mode, as applicable. The trigger/gate signal must be +2V, but less than ±50V. Input impedance is 1 kΩ. In triggered mode, the trigger signal will cause one cycle of output at the 50Ω OUT connector; in gate mode, the trigger signal will cause an integral burst of cycles lasting for the duration of the trigger signal plus the time required to complete the last cycle initiated during the trigger signal.

3.3.4 Operating as a DC Voltage Source

DC voltage output is not specified, but ±5V, 100 mA may be obtained by using offset voltage referred to the 0V level of the 50Ω OUT during the nontrigger time of trigger mode.

1. Terminate the 50Ω OUT connector with a 50Ω ±0.1% termination.
2. Select ∿ function and trigger mode.
3. Program 9.99 X 10^1 frequency.
4. Program 0.00 X 10^0 amplitude.
5. Ensure that no trigger signals are received.
6. Select the desired dc output by programming it as offset voltage.

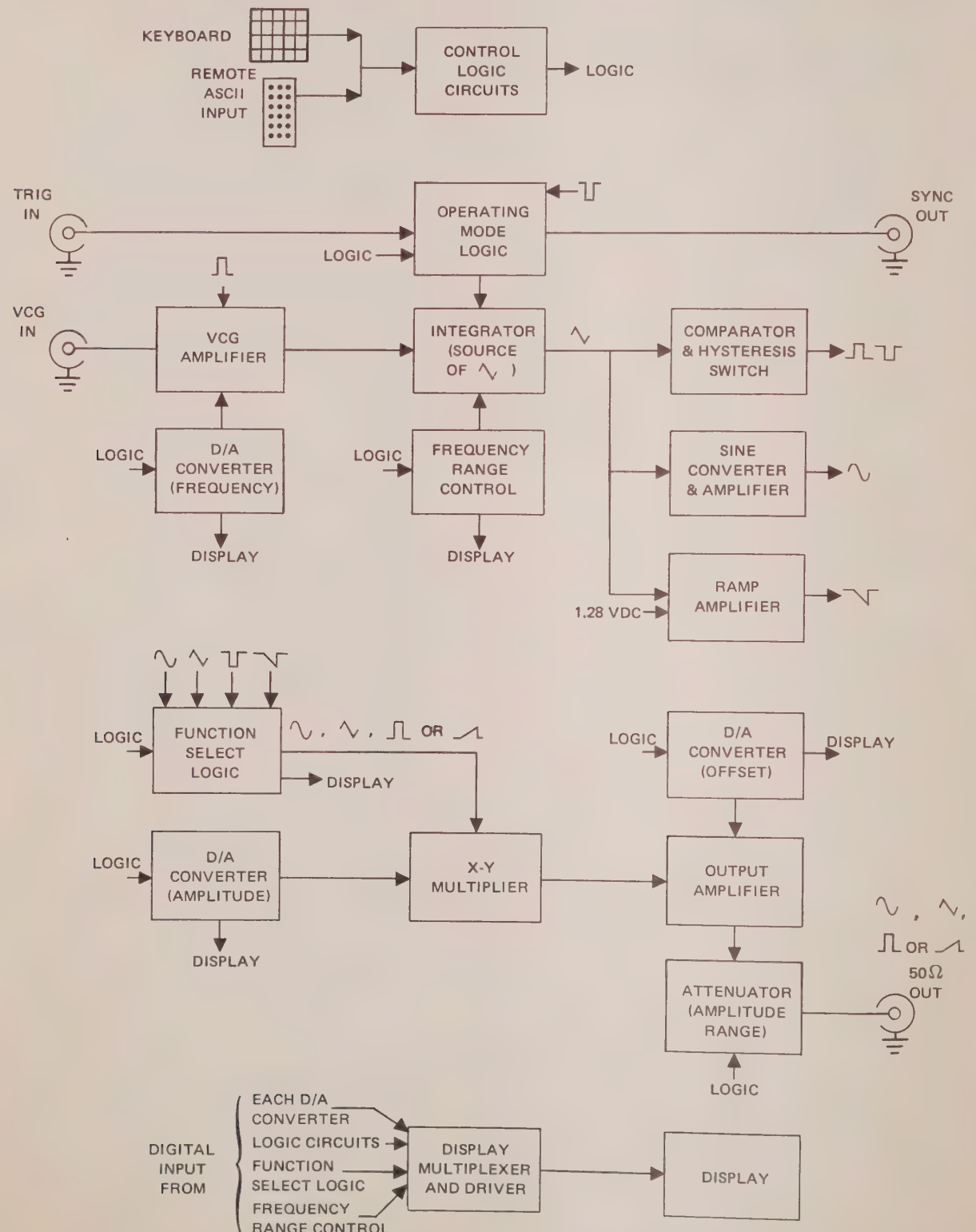


Figure 4-1. Overall Block Diagram

SECTION 4
CIRCUIT DESCRIPTION

4.1 LOGIC NOTATION AND TERMINOLOGY

To avoid confusion in determining logic states, please read and understand the following ground rules used in this manual.

1. On the schematics, all signals are true when high unless their mnemonics are overscored; the overscore indicates true-when-low.

2. Pulse and clock refer to transient change of state, whereas status refers to a logic state which requires new input to change.

4.2 BASIC OPERATION

The overall operation can be easily followed in Figure 4-1. All digital programmed inputs are via the keyboard or the remote ASCII connector. Two input BNC connectors are for the TRIG IN and VCG (voltage control of generator) IN signals. The outputs are selectable ∿ , ∿ , ⎍ or ⟋ waveform at the 50Ω OUT BNC. A sync output BNC is also provided for a TTL compatible square wave.

The integrator and comparator and hysteresis switch, acting upon each other, generate the basic waveforms of square and triangle. The mode of operation (triggered, gated or continuous) is logic controlled to act upon the integrator. Logic controls capacitance for generator frequency range and current, via a D/A converter and VCG amplifier, for specific frequency in the selected range. VCG IN voltage will also control frequency.

Diode arrays in the sine converter form the sine wave, and the square wave multiplexes the triangle wave and a voltage level to form the ramp waveform.

The waveform to be output is selected and multiplied with the selected amplitude, after which it is offset and attenuated as programmed.

The digital control data is multiplexed into the display bus for display panel illumination.

4.3 INPUT/OUTPUT

Seven-bit ASCII characters (see Table 2-2 and Drawing 158-200) and clock pulses are supplied to an ASCII data bus on the digital board thru the ASCII DATA IN/OUT connector or supplied by the keyboard to the digital board. (Generators with options will accept and convert other data formats. Once converted, the data is placed on the ASCII data bus.) The character bits are 0 to 0.4 volt for a binary 1 and $\geq$ 2.4V, $<$ 5.0V or open for a binary 0. The character bits are designated D0 thru D6 and prefixed as to their type; i.e., X for in/out external, K for keyboard, and OPT for optional interface conversion.

The ASCII data bus is that set of eight lines handling D0 thru D6 and CLK. Keyboard input J2 is always a part of the bus as well as the termination socket XIC41 (shown in Drawing 158-218, Sheet 1).

Non-ASCII signals to the generator are VCG IN, which is connected to the analog board via the digital board, and TRIG IN, which goes to the trigger logic on the digital board. The generator main output signal is from the analog board to the rear panel 50Ω OUT BNC connector; this signal is a selectable ∿ , ∿ , ⎍ or ⟋ that can be offset, inverted and varied in amplitude. The SYNC OUT signal is a fixed amplitude square wave that is TTL compatible.

4.4 INTERFACE (Drawing 158-218, Sheet 1)

By means of jumpers (Drawing 158-218, Sheet 1), the standard model signals bypass the option card connector J4, allowing J9 (ASCII DATA IN/OUT) to be connected directly to the ASCII data bus. The ASCII data bus may extend thru several instruments. In any case, the integrated circuit termination pack should be inserted only once on the ASCII data bus and at the far end of the bus from the keyboard or control device.

4.5 KEYBOARD (Drawing 159-216)

The keyboard transmits pressed-key data plus a clock pulse to the ASCII data bus. Proper time alignment of the seven data bits and clock is maintained by the IC9 clock circuit driving IC5, a binary counter, to generate a time code. The

counter and the decoder chips (IC3 and IC7C) select a column of keys that are scanned by the multiplexer IC4 to generate time "windows" for the data bits corresponding to each key function. IC4 outputs transmit the status of the selected input. For example, between IC5 count 0 and 1, a 7-bit code for key 0 is generated and ready to be placed on the ASCII data bus if the 0 key is pressed. If the key is pressed, the binary counter IC5 stops and the seven bits plus a clock pulse are placed on the data bus. When the key is released, the windows for keys 1, 2, 3, etc., are generated in sequence.

4.6 DIGITAL BOARD CONTROL LOGIC (Drawing 158-218, Sheet 2)

The stream of ASCII characters (seven parallel bits per character) is decoded into hexadecimal data. This data is then distributed throughout logic control circuitry to program all of the holding registers which control the operation of the generator. Refer to Table 2-2 for conversion of programmed signals, keyboard, hexadecimal, binary and logic bit terminology.

Four types of clock pulses are generated to categorize the bits of data: alpha clock, numerals clock, minus sign clock and range clock. These clock signals, along with the data bits, cause explicit control signals to be generated.

Control logic consists of the following collection of logic blocks:

1. Binary to hexadecimal conversion (0 thru 9, D, 20, 30 and 40)
2. Unit Enable (ITSME)
3. Minus Sign Clock (MCLK)
4. Alpha (Except Multiplier) Clock (40EC)
5. Numerals Clock (30C)
6. Numeral Enables
7. Range (X 10 Multiplier) Clock (RNGCLK)
8. Display Digits Reset (ADRSET)
9. Minus Sign Enable (MSIGN)
10. On/Off Control (ENABLE)
11. Two-Star Converter (D0* thru D3*)
12. Turn-On Reset (RESA, RESB)
13. Trigger Clock (TRIGC)
14. Mode Select (M0, M1)
15. Manual Trigger
16. Generator Enable ($\overline{\text{OPERATE}}$)
17. Function Select (F0, F1)

4.6.1 Binary to Hexadecimal Conversion (0 thru 9, D, 20, 30 and 40)

The seven bits of character and one clock bit are converted to hexadecimal code. The four least significant bits are converted to a decimal number from 0 thru 9 or D. The three most significant bits are converted to 20, 30 or 40 and enabled for the duration of the clock pulse. See the hexadecimal column in Table 2-2. As shown in the table, 2D is ASCII minus and 20 is ASCII space. Then, on the schematic 20 with D is minus and 20 with 0 is space (the space is one of two multiplier addresses). Hexadecimal 30 with 0 thru 9 are the result of numeric data, and hexadecimal 40 with 0 thru 9 are the result of alpha data.

4.6.2 Unit Enable (ITSME)

A jumper from E24 or E25, etc., to E29 determines the address of the generator as 1, 2, etc. When unit select and a number are programmed, and the number is the correct unit address, ITSME status is generated. ITSME enables alpha and numerals clock and the display.

4.6.3 Minus Sign Clock (MCLK)

MCLK is generated when a phase inversion or negative offset is programmed (ASCII –).

4.6.4 Alpha (Except Multiplier) Clock (40EC)

If the correct generator is addressed and any alpha other than multiplier is input, a clock pulse is generated (40EC and $\overline{\text{40EC}}$). This signal is used to clock all alpha related functions except the range (or X 10 multiplier). $\overline{\text{ITSME}}$ enables.

4.6.5 Numerals Clock (30C)

Numerals clock (30C) is used to distinguish between alphas

and numerics and to clock numeric related functions.

4.6.6 Numeral Enables

This circuit triggers the display digit reset one-shot and enables a portion of the range clock circuit only for the numeral programmed immediately after an alpha (except range). Output is

Numeral = High
Alpha = Low

4.6.7 Range (X 10 Multiplier) Clock (RNGCLK)

If a numeral was last programmed, an ASCII space programmed will generate a range clock pulse (RNGCLK). Or, if range (ASCII E) is programmed, a range clock pulse is generated. This pulse is used to set the range gate to enable the frequency range logic and the amplitude attenuator logic.

4.6.8 Display Digits Reset (ADRSET)

A high following a low from the numerals enable circuit triggers a 100 ns ADRSET pulse. This pulse is used to clear the registers for the display digits. Therefore, a numeral programmed after an alpha, such as frequency or amplitude, causes the registers to be cleared, but another programmed numeral will not cause the registers to clear.

4.6.9 Minus Sign Enable (MSIGN)

MSIGN status is generated on the falling edge of MCLK; that is, an inverted phase or offset has been programmed. MSIGN status is removed when an alpha is generated. MSIGN is used to change the polarity of the amplitude or offset.

4.6.10 On/Off Control (ENABLE)

The 50Ω OUT output is enabled when output-on is programmed. Output-on (ASCII H) generates ENABLE and $\overline{\text{ENABLE}}$. Output-off (ASCII I) inhibits ENABLE and $\overline{\text{ENABLE}}$.

4.6.11 Two-Star Converter

	Decimal									
	0	1	2	3	4	5	6	7	8	9
XD0		H		H		H		H		H
XD1			H	H			H	H		
XD2					H	H	H	H		
XD3									H	H
XD0*		H		H		H		H		H
XD1*			H	H			H	H	H	H
XD2*					H	H	H	H	H	H
XD3*									H	H

4.6.12 Turn-On Reset (RESA, RESB)

This one-shot multivibrator clears or presets all necessary holding registers at power-on time.

4.6.13 Trigger Clock (TRIGC)

When the operating mode is programmed (ASCII B), the gate IC49 is enabled in order for the following programmed numerals clock pulse (30C) to generate the trigger clock pulse ($\overline{\text{TRIGC}}$). This pulse is used to gate the manual trigger D0 binary data bit and clock bits $\overline{1}$ and $\overline{2}$ of mode numerics at the mode select circuit to generate M0 and M1.

4.6.14 Mode Select (M0, M1)

$\overline{1}$	$\overline{2}$	MODE	M0	M1
H	H	CONT	L	L
L	H	TRIG	H	L
H	L	GATE	L	H

Numerics $\overline{1}$ and $\overline{2}$ determine status of M0 and M1 when clocked by $\overline{\text{TRIGC}}$. These status signals define the operating mode of the generator in the trigger circuit and display.

4.6.15 Manual Trigger

After the trigger mode is programmed, any subsequent programmed ASCII binary bit D0, such as the numeral 1, will generate another $\overline{\text{TRIGC}}$; the combination of $\overline{\text{TRIGC}}$ and D0 is a manual trigger pulse. The manual trigger rate must be slower than the generator frequency.

4.6.16 Generator Enable ($\overline{\text{OPERATE}}$)

See Paragraph 4.6.14 for M0 and M1 status for a given mode.

Continuous Mode. If continuous mode is programmed, M0 and M1 are low which holds $\overline{\text{OPERATE}}$ low, allowing the generator to run.

Gated Mode. In gated mode, M0 is low and M1 is high. Trig-mode gate is held high; gate-mode gate is gated and will respond to a trigger signal. When TRIG is high, $\overline{\text{OPERATE}}$ is low. When TRIG is low, the low is removed from the IC40B clear, and the completion of the SQR square wave at the IC40B clock input causes $\overline{\text{OPERATE}}$ to be high.

Triggered Mode. In triggered mode, M0 is high and M1 is low. Gated-mode gate is held high; trig-mode gate is gated and will respond to the TRIG or manual trigger signal. A trigger causes the trig-mode gate to go high, allowing $\overline{\text{OPERATE}}$ to be low. $\overline{\text{OPERATE}}$ feedback to IC40A removes the clear on IC40B and upon the completion of the SQR square wave at the IC40B clock input causes $\overline{\text{OPERATE}}$ to go high.

4.6.17 Function Select (F0, F1)

When the alpha for function is programmed (ASCII C), the gate IC49 is enabled in order for the following programmed numerals clock pulse (30C) to clock ASCII binary bits D0 and D1. D0 and D1 are the least significant bits of the programmed numeral. (0 = ∿ , 1 = ⩘ , 2 = ⎍ and 3 = ⩘ .) Outputs are as noted on the schematic.

4.7 FREQUENCY D/A LOGIC (Drawing 518-218, Sheet 6)

The programming of the frequency alpha (ASCII F) enables the clearing and clocking gates for the frequency numeric data holding registers. The programming of a numeral following the frequency alpha will clear the registers and enter the data in the LSD register. Subsequent programmed numerals will be entered serially without any clearing action. Output data of the registers controls the diode gates, which switch current thru weighting resistors into a summing node of an amplifier to create the analog voltage labeled D/F. The register output data is also used for display information.

If the range alpha (ASCII E) is programmed and frequency was the last programmed alpha, the frequency clearing and clocking gates are disabled and the gate for the range data holding register is enabled. Subsequent programmed numerals will enter the data at the range data holding register input. The outputs FR0, FR1 and FR2 of this register are decoded to decimal data which are used to control relays for selected range capacitors and frequency adjustment controls (see Schematic 158-219 and Paragraph 4.12.5). FR0, FR1 and FR2 are also used as display information.

4.8 OFFSET D/A LOGIC (Drawing 158-218, Sheet 5)

The programming of the offset alpha (ASCII D) enables the clearing and clocking gates for the offset numeric data holding registers. The programming of a numeral following the offset alpha will clear the registers and enter data in the LSD register. Subsequent programmed numerals will be entered serially without any clearing action. Output data of the registers controls the diode gates, which switch current thru weighting resistors into a summing node of an amplifier to create the analog voltage labeled DC OFFSET. The register output data is also used for display information.

If inversion is programmed (ASCII –) following offset, MOFFSET is generated which causes the electronic SPDT switch to control the polarity of the selected offset voltage.

4.9 AMPLITUDE D/A LOGIC (Drawing 518-218, Sheet 4)

The programming of the amplitude alpha (ASCII A) enables the clearing and clocking gates for the amplitude numeric data holding registers. The programming of a numeral following the amplitude alpha will clear the registers and enter the data in the LSD register. Subsequent programmed numerals will be entered serially without any clearing action. The output data of the registers controls the diode gates, which switch current thru weighting resistors into a summing node of an amplifier to create the analog voltage labeled D/V. The register output data is also used at the display driver circuit.

If the range alpha (ASCII E) is programmed and amplitude was the last programmed alpha, the frequency clearing and clocking gates are disabled and the gate for the range data holding registers clock is enabled. Subsequent programmed numerals will enter numeric data at the range data holding register inputs with the following results:

$\overline{1}$	$\overline{2}$	–20 dB	–40 dB	0 dB
H	L	L	H	L
H	H	L	L	H
L	H	H	L	L

Where 0 dB = X 10^0 multiplier
–20 dB = X 10^{-1} multiplier
–40 dB = X 10^{-2} multiplier

Normal waveform phase has been set by the function select circuit signal F1 in the following manner:

Function	F1	MAMPL	Q7	Q8	Normal-Phase D/V Polarity
∿	L	L	On	Off	+
⩘	L	L	On	Off	+
⎍	H	H	Off	On	–
⩘	H	H	Off	On	–

If inversion is programmed (ASCII –) following the amplitude alpha, MAMPL status is reversed, causing the electronic DPST switch controlling Q7 and Q8 to reverse the polarity of the analog signal D/V. D/V controls 50Ω OUT signal amplitude and polarity at the X-Y multiplier (see Schematic 518-219 and Paragraph 4.12.7).

4.10 DIGITAL BOARD DISPLAY (DRIVER) LOGIC (Schematic 158-218, Sheet 3)

All of the status data from the holding registers are accumulated and multiplexed into the display logic. By multiplexing, the data is transferred to the display in a minimum amount of lines (DD0 thru DD3) and then is decoded on the display board. To synchronize the transferred data, a sync ($\overline{\text{DSYNC}}$) line and clock ($\overline{\text{DCLK}}$) pulse are provided for both multiplexing and decoding.

4.10.1 Clock and Multiplex Time Code

The divide-by-9 binary counter IC37, clocked at a 5 kHz rate, supplies the necessary time codes (K0, K1, K2, K3) for multiplexing the display data. The same 5 kHz clock also drives the clock pulse DCLK for the display.

4.10.2 Select Frequency, Amplitude or Offset Display

$\overline{\text{SELF}}$	$\overline{\text{SELA}}$	$\overline{\text{SELOFF}}$	SD0	$\overline{\text{SD0}}$	SD1	$\overline{\text{SD1}}$
L	H	H	H	L	L	H
H	L	H	L	H	L	H
H	H	L	L	H	H	L

The SELF, SELA and SELOFF status signals from their respective D/A circuits generate the SD0 and SD1 codes which enable frequency, amplitude, offset, range or minus sign data for multiplexing. Because amplitude, frequency and offset share the same numerical display, this code necessarily ensures that only one set of data is enabled at a time.

4.10.3 Amplitude, Frequency and Offset Multiplexing

All three of the multiplexer outputs are paralleled and connected to the display bus thru the 2-star decoder. The three multiplexer chips, frequency, amplitude and offset, receive input data from the holding registers of their respective D/A converters. The multiplexers are enabled by the programming of frequency, amplitude or offset, which generate SD0 and SD1, and by time code $\overline{\text{K2}}$. In a specific multiplexer, the three groups (A, B and C) of four data bits each are placed on the bus (DD0, DD1, DD2 and DD3) by time codes K0 and K1. See the chart on the schematic and the ABC versus K0, K1 matrix on the multiplexer itself for logic and states and timing. The 2-star decoder converts the 2-star bit weighting back to conventional binary (see 2-star converter, Paragraph 4.6.11).

4.10.4 Amplitude and Frequency Range (X 10 Multiplier) Multiplexing

In the multiplexer A groups, −20 and −40 dB are amplitude attenuation, while FR bits of the B group are frequency selection bits. The A group or the B group is enabled for multiplexing by SD0, which is high for frequency display and low for amplitude and offset. Multiplexing is controlled by time codes $\overline{\text{K0}}$, $\overline{\text{K1}}$ and $\overline{\text{K2}}$ (see the chart on the schematic).

4.10.5 Minus Signs, Function and Enable, and Mode and Unit Select Multiplexing

Multiplexing of the following signals is controlled by K2, $\overline{\text{K0}}$ and $\overline{\text{K1}}$, as shown on the schematic chart.

The minus sign for amplitude is gated by the selection of amplitude for display, $\overline{\text{SD1}}$ and $\overline{\text{SD0}}$ high. The minus sign for offset is gated by the selection of offset for display, $\overline{\text{SD0}}$ and SD1 high. 0 dB or SD0 high (the selection of frequency) will be used to inhibit the range minus sign for frequency and 0 dB amplitude. SD0 and SD1 states are used to light the display mode LEDs. F0 and F1 states are used to light the function (waveform) LEDs. $\overline{\text{ENABLE}}$ is used to enable the display of the function symbol. M0 and M1 states cause the operating mode LEDs to light. ITSME causes the UNIT SELECTED LED to light.

4.10.6 Display Enable

Some systems may have several instruments connected to one display. Display enable ensures that only one instrument at a time drives the display. If this unit is selected ($\overline{\text{ITSME}}$), its display data will be gated. If it is not selected, but power is on, the subsequent K3 edge will cause a low to be generated, disabling the display data output.

4.11 DISPLAY LOGIC (Drawing D158-217)

The display board receives the multiplexed data character (bits DD0 thru DD3) from the digital board. At each character time, the bits represent one of the following display items or groups:

Data	Display	Enable Signal	Data Bits
Range Digit	DS1	DIG9	DD0 - DD3
Most Significant Digit	DS2	DIG1	DD0 - DD3
Middle Digit	DS3	DIG2	DD0 - DD3
Least Significant Digit	DS4	DIG3	DD0 - DD3
Display Mode	CR11 - CR13	DIG4	DD2 - DD3
3-Digit-Value Minus Sign	DS8	DIG4	DD0
X 10 Multiplier Minus Sign	DS7	DIG4	DD1
Function (Waveform)	CR1 - CR4	DIG5	DD0 - DD3
Operating Mode	CR8 - CR10	DIG6	DD0 - DD2
Unit Select	CR17	DIG6	DD3

The routing of the correct data to the correct display is determined by the clock pulse shifting the XSYNC bit thru the 9-bit parallel output shift register. The shift register outputs (DIG1 thru DIG9) enable the clock signal to clock the multiplexed data bits into the proper display holding registers at the proper time, thus correctly routing and de-skewing the data bits.

4.12 ANALOG BOARD (Drawing 158-219)

4.12.1 Generator Loop

The purpose of this loop is to generate symmetrical triangle and square waves simultaneously.

Control of current direction for capacitor C (Figure 4-2) charging is determined by whether diode switch CR1 (IC14-7) is forward biased (turned on) or reverse biased (turned off). Resistors R22, R40, R45, R52, R58 and R73 are matched to ensure equal currents.

When the voltage at point A is positive, diode CR1 is forward biased and CR2 is reverse biased. When CR1 is forward biased by the positive cycle of the square wave, current 2I (twice I) pulled by the 1st VCG amplifier comes from the square wave source. Because CR2 (IC14-6) is reverse biased, the current I from the 2nd VCG amplifier is charging the capacitor C which causes the voltage at point B to decrease linearly. As soon as the voltage at point B reaches −1.25V, the output of the hysteresis switch will switch to a negative voltage. CR1 becomes reverse biased and CR2 becomes forward biased. The current pulled by the 1st VCG amplifier (2I) is now comprised of the current from the 2nd VCG amplifier (1I) and exactly 1I from the capacitor C, which is the same amount as its charging current. The voltage at point B will increase. Again the hysteresis will switch positive when the voltage at point B reaches +1.25V. Thus, the triangle and square wave signals are generated simultaneously.

4.12.2 VCG Amplifier

The output frequency depends on the size of the capacitor selected and the amount of current I charging the capacitor. The magnitude of the current is controlled by the VCG amplifiers, which in turn are controlled by the voltage from the frequency D/A amplifier and the VCG input.

4.12.3 Sine Converter and Amplifier

The triangle is shaped into a sine wave thru three diode networks utilizing the nonlinearity of the diodes. The outputs of these diode networks are summed and amplified in the sine amplifier.

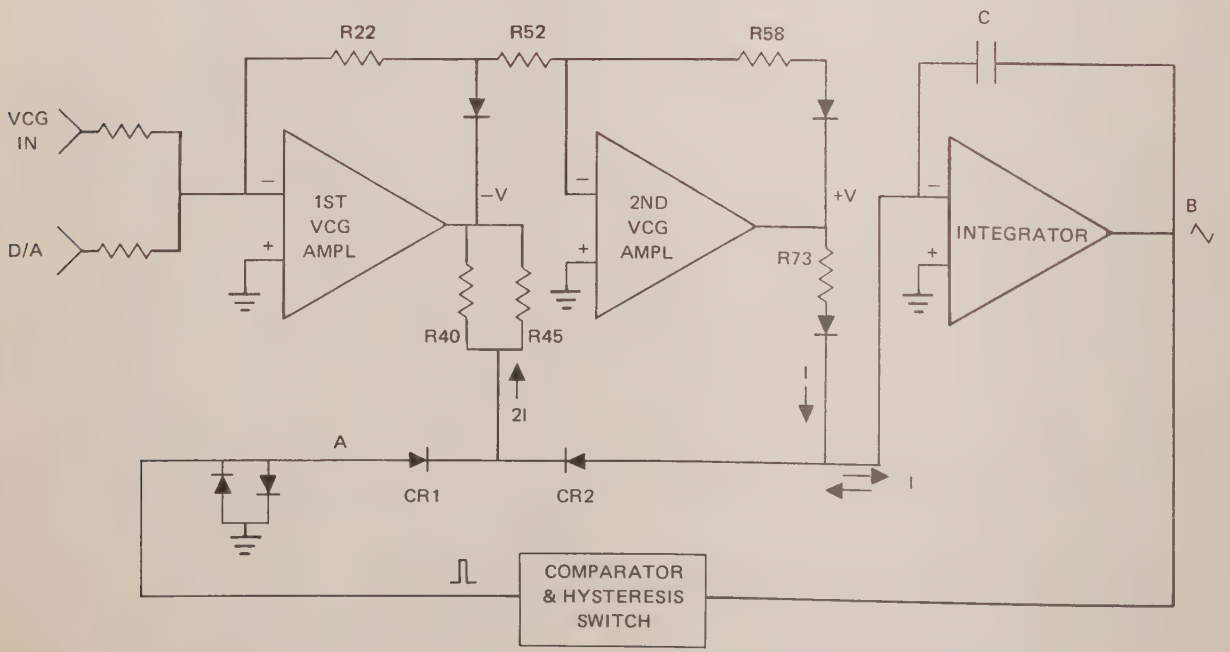


Figure 4-2. Generator Loop

4.12.4 Ramp Amplifier

A square wave from the comparator circuit (Figure 4-3) alternately enables the negative triangle ramp thru IC8A and the +1.25V from R64 thru IC8B to form the ramp waveform. The output resultant is +1.25V during one half cycle and the negative going portion of the triangle during the other half portion.

4.12.5 Frequency Range Logic

FR0	FR1	FR2	Power of 10
L	L	L	0
H	L	L	1
L	H	L	2
H	H	L	3
L	L	H	4
H	L	H	5
L	H	H	6
H	H	H	7

This circuit contains a binary to decimal decoder, which converts three lines of input data (FR0, FR1, FR2) to a one-line-of-eight output in order to drive the frequency range multiplier relays and control adjustments. FR0, FR1 and FR2 originate from holding register IC23 on the digital board (see Frequency D/A Logic, Paragraph 4.7).

4.12.6 Function Selector

$\overline{F0}$	$\overline{F1}$	Function
H	H	∿
L	H	∿
H	L	⎍
L	L	◿

Selection of each waveform is accomplished by electronic switches. See Digital Board Schematic 158-218, Sheet 2, and Paragraph 4.6.17 for the origin of $\overline{F0}$ and $\overline{F1}$.

4.12.7 X-Y Multiplier and Output Amplifier

The selected waveform is fed into one input of the X-Y multiplier and a control voltage from the amplitude D/A amplifier is fed to the other input. Refer to Figure 4-4. The differential output from the X-Y multiplier is directly proportional to the product of the two inputs. One of the differential outputs is fed thru an inverting amplifier and then summed into a second inverting amplifier along with the other differential output from the x-y multiplier. The combined operation of these two inverting amplifiers is equal to one differential amplifier. Waveform inversion and addition is as shown in Figure 4-4.

4.12.8 Attenuator Select Logic

Attenuation of 0 dB, −20 dB or −40 dB is accomplished by selecting one-of-three range relays and an enable relay allowing the output amplifier to be enabled or disabled to the 50Ω OUT connector.

4.12.9 Generator Enable

The triangle generator loop will free run continuously only if the $\overline{OPERATE}$ voltage is low. Refer to Figure 4-5. When the $\overline{OPERATE}$ voltage is high, the output of the integrator will be clamped to the input, which stops the generator from free running. The J-K flip-flop is used to control the timing so that the triangle will always stop at the end of the cycle. The triangle will stop at time t_3 if $\overline{GATE\ ENABLE}$ is reset high between times t_1 and t_2 as shown in the timing diagram of Figure 4-5. $\overline{OPERATE}$ originates from the digital board generator enable circuit (refer to Schematic 158-218, Sheet 2, and Paragraph 4.6.16).

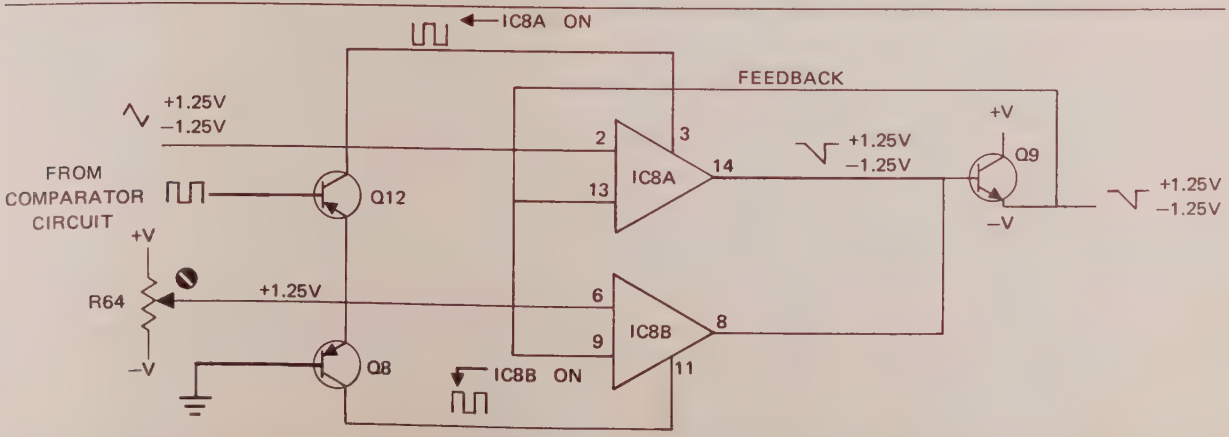


Figure 4-3. Ramp Amplifier

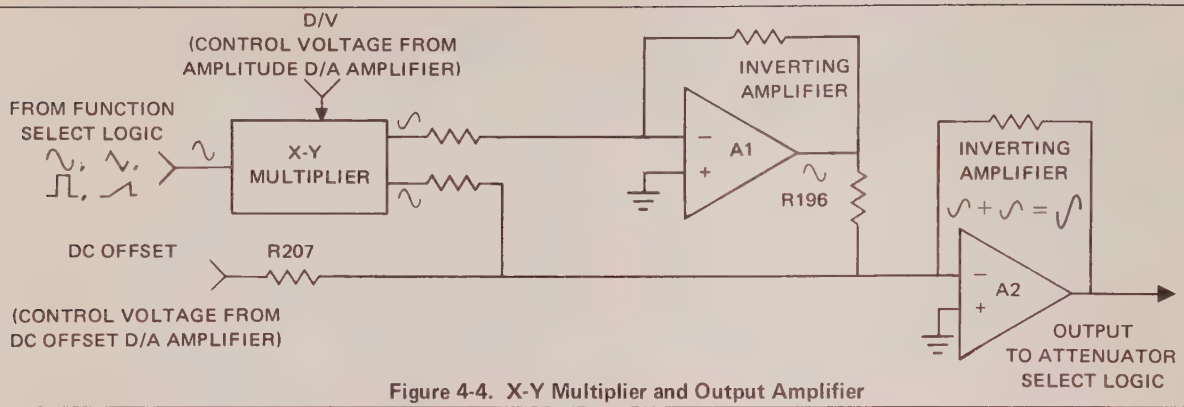


Figure 4-4. X-Y Multiplier and Output Amplifier

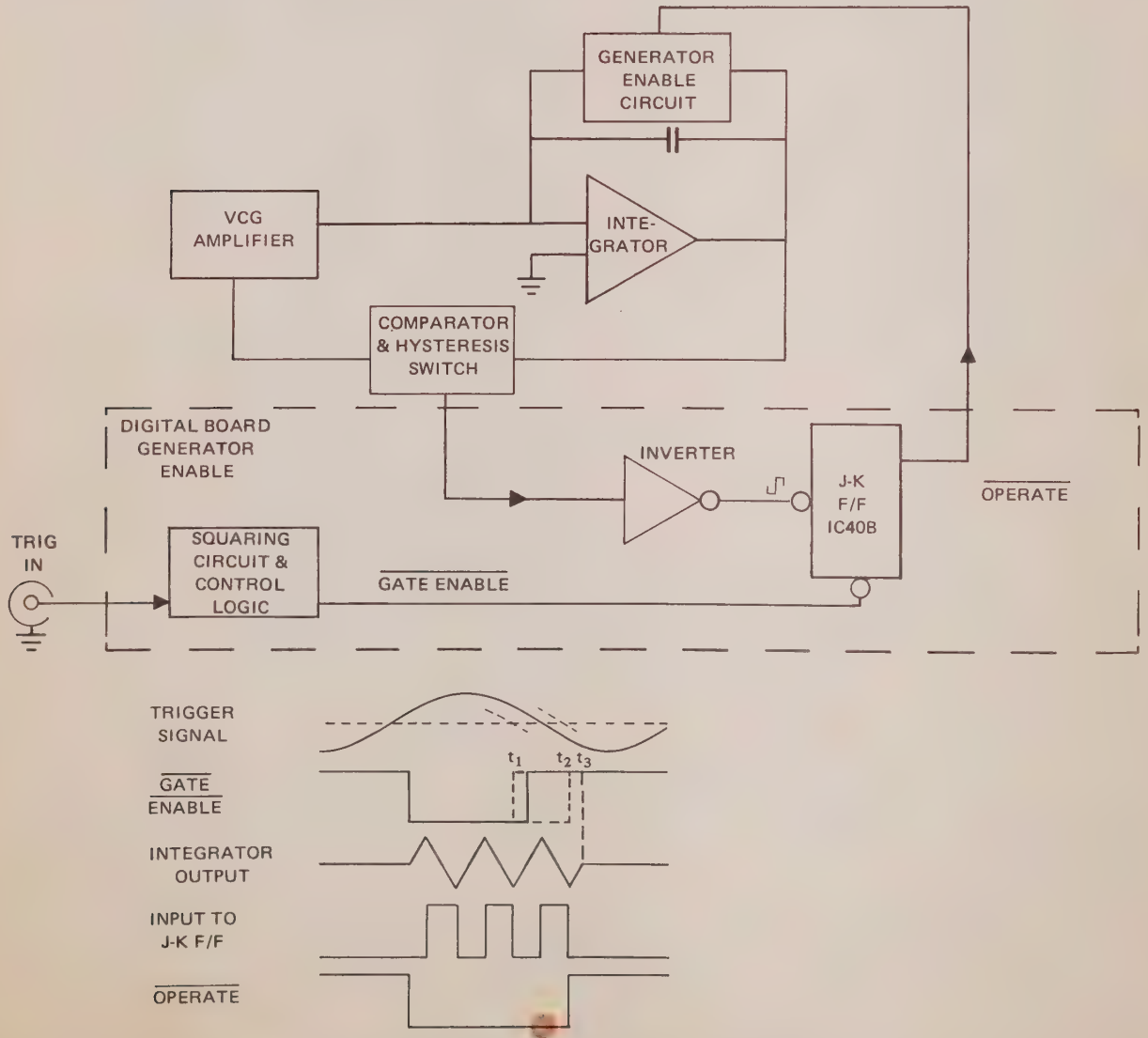


Figure 4-5. Trigger/Gate Block and Timing Diagrams

SECTION 5
CALIBRATION

After referring to the following preliminary data, perform calibration, as necessary, per Table 5-1. If performing partial calibration, check previous settings and adjustments for applicability.

1. Refer to calibration drawing, Figure 5-2, and calibration chart (Table 5-1).

2. Unless otherwise noted, all measurements made at the 50Ω OUT connector should be terminated into a 50Ω (±0.1%) load.

3. TPs (Test Points) and adjustments are prefixed as follows:

   A1 – Power Supply
   A2 – Digital Board
   A3 – Analog Board

4. Before connecting the unit to an ac source, check the ac line circuit to make sure the 115/230 and HI/LO switches are set at the correct position (see Paragraph 2.2.1).

5. Start the calibration by setting the front panel switches or program for the following:

Power . . . . . On
Unit Select . . . . . Select unit to be calibrated
Mode . . . . . Continuous
Frequency 9.99E2
Amplitude 9.99E0
Offset 0.00
Function . . . . . ∿
Output On/Off . . . . . On

6. Allow the unit to warm up at least 30 minutes for final calibration.

Table 5-1. CALIBRATION CHART

Check	Tester	Calibrated Points	Program	Seq	Control	Desired Results	Remarks
Power Supply Regulation	Voltmeter	A3TP2 (+15V), A3TP1 (Gnd)	See initial conditions.	1	A1R24	+15V ±20 mV	
		A3TP3 (–15V), A3TP1		2	–	–15V ±50 mV	
		A3TP4 (+5V), A3TP1		3	–	+5V ±250 mV	
Triangle Amplitude 5%	Oscilloscope	A3TP5, A3TP1 (Gnd)		4	A3R59	+1.25V ±5 mV	Impossible Use 7A13 Plug IN
		A3TP5, A3TP1		5	A3R62	–1.25V ±5 mV	
Symmetry	Oscilloscope	50Ω OUT	Func ⎍ Freq 0.10E4 See Board for Action of each adj	6	A3R16	Minimum frequency change*	*While opening and shorting VCG IN to BNC case.
				7	A3R90, A3R17*	Time symmetry error <1%	*Use if necessary for adjustment of proper frequency.
			Freq 0.01E4	8	A3R44, A3R17*	Time symmetry error <1%	*Use if necessary for adjustment of proper frequency. Repeat 7 and 8, as necessary, for optimum results.

Table 5-1. CALIBRATION CHART (Continued)

Check	Tester	Calibrated Points	Program	Seq	Control	Desired Results	Remarks
Frequency	Counter	SYNC OUT	Freq 9.99E3	9	A3R2	9.99 kHz	
			9.99E5	10	A3C33	999 kHz	
			1.00E3	11	A3R17	1.00 kHz	Repeat 9, 10 and 11 for optimum results.
			0.00E3	12	A3R17	<10 Hz	If adjustment is made, repeat 11.
			9.99E0	13	A3R15	9.99 Hz	
			9.99E1	14	A3R11	99.9 Hz	
			9.99E2	15	A3R6	999 Hz	
			9.99E4	16	A3C15	99.9 kHz	
			3.00E6	17	A3R5	3.00 MHz	
			1.00E6	18	A3R5	1.00 MHz	Repeat 17 and 18 for optimum results.
X-Y Multiplier	Oscilloscope	A3TP5, A3TP1 (Gnd)	Func ∿ Freq 9.99E2 Ampl 0.00E0 Ofst 0.00 Mode Trig	19	A3R119	0V ±5 mV	
		50Ω OUT	Short A3TP5 to A3TP1	20	A2R28	Minimum voltage shift (±5 mV)	Obtain minimum voltage shift when switching between + and − offset. Adjust A3R217 to keep voltage at zero.
			Ampl 0.00	21	A3R182	<10 mV	
			Ampl 9.99	22	A3R182	<10 mV	Recheck 21. Readjust A3R217 to keep voltage at zero.
			Remove A3TP5 short Ampl 0.00E0 Mode Cont	23	A3R186	Minimum signal	
			Ampl 0.02E0	24	A3R201	Most linear triangle waveform	
			Ampl 0.00E0	25	A2R186, A2R99	Minimum + and − amplitude	Obtain minimum signal in both + and − amplitude.

Table 5-1. CALIBRATION CHART (Continued)

Check	Tester	Calibrated Points	Program	Seq	Control	Desired Results	Remarks
Sine Distortion	Oscilloscope, LF Sine Distortion Amplifier with X 1 probe	A3TP5*	Func ∿ Ampl 9.00E0	26	A3R137, A3R138	Minimum sine distortion	*See Figure 5-1 for test setup.
		50Ω OUT		27	A3R190	Minimum sine distortion	Typically <0.2%. See Figure 5-1 for test setup.
			Freq* 9.99E3 9.99E2	28	A3R137, A3R138, A3R190	Minimum sine distortion	*Optimize for both settings.
				29			Repeat 19 thru 23.
Output Amplitude and DC Offset	Voltmeter	50Ω OUT	Short A3TP5 to A3TP1 Func ∿ Ampl 0.00E0 Ofst 5.00 Mode Trig	30	A2R30	+5.00 Vdc ±10 mV	
			Ofst –5.00	31	A2R34	–5.00 Vdc ±10 mV	
			Ofst 0.00	32	A2R28	Minimum voltage shift (<5 mV)*	*While switching from + and – dc offset. Adjust A3R217 to keep voltage at zero.
				33			Repeat 30, 31 and 32 to optimize.
		Freq. 9.99E2	Remove A3TP5 short Ampl 9.99E0 Mode Cont	34	A2R107	9.99V p-p ∿ ±10 mV	
			Ampl–9.99E0	35	A2R111	9.99V p-p ∿ ±10 mV	
			Func ⎍ Ampl 9.99E0	36	A3R55, A3R48	±5.00V peak ±10 mV	
			Ampl–9.99E0	37	A3R55, A3R48	50% of observed error*	*Split error with 36.
			Func ∿	38	A3R98, A3R116	±5.00V peak ±10 mV	R98 - Amplitude R116 - Symmetry
			Func ◿	39	A3R79, A3R64	±5.00V peak ±10 mV	R79 - Symmetry R64 - Separation

Table 5-1. CALIBRATION CHART (Continued)

Check	Tester	Calibrated Points	Program	Seq	Control	Desired Results	Remarks
Output Amplitude and DC Offset (Continued)			Func ⎍ Freq 9.99E5 Ampl 1.00E0	40	A3C53, A3C56	Best square wave in both + and − amplitude	

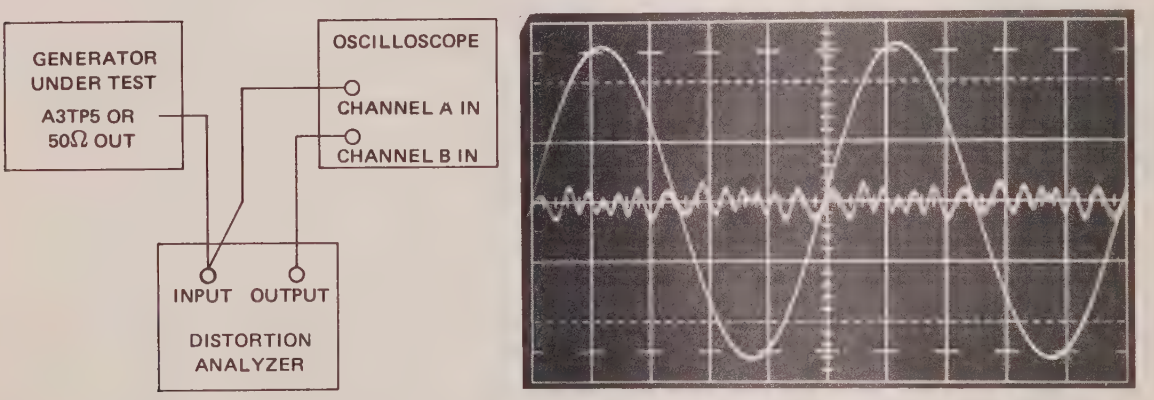
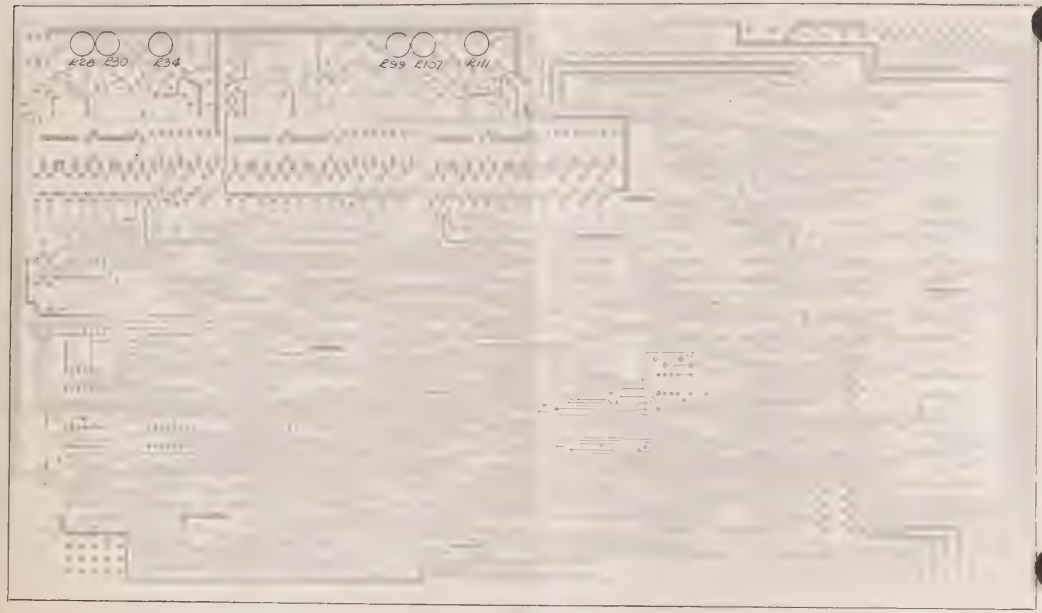
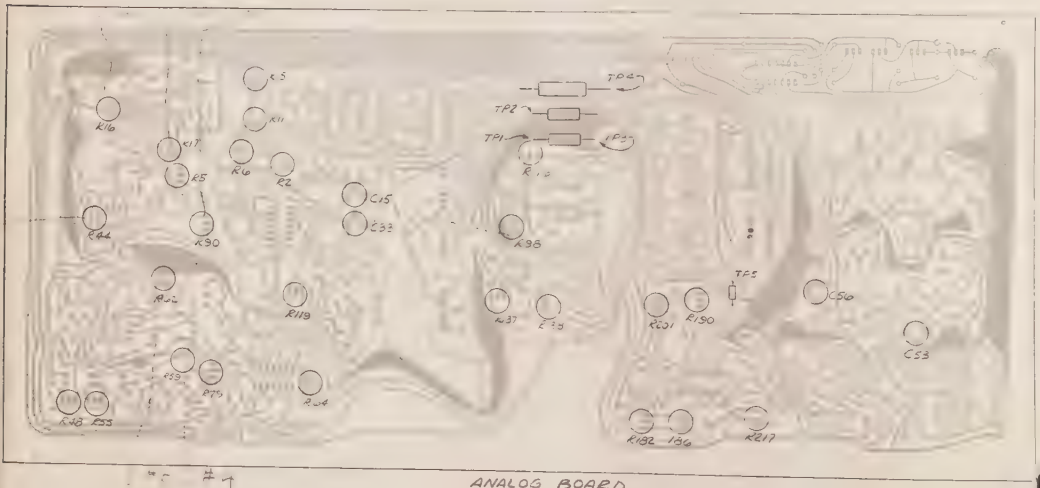


Figure 5-1. Distortion Analysis Test Setup



DIGITAL BOARD



ANALOG BOARD

Figure 5-2. Calibration Drawing

SECTION 6
TROUBLESHOOTING

6.1 CORRECTIVE MAINTENANCE

This portion of the manual presents a systematic approach to troubleshooting. It is composed of three parts:

Part 1. Troubleshooting Techniques for Individual Components (Paragraph 6.2) — Frequently you can quickly locate a defective component by this technique without understanding the detailed function of the circuit. It is also a necessary technique when extensive troubleshooting in the component level is required.

Part 2. Quick Troubleshooting Guide (Paragraph 6.3) — Start by observing the symptoms of malfunctioning; then use the guide to find the defective components or malfunctioning circuits.

Part 3. Key Signals, Voltages and States (Table 6-1) — This is a supplemental procedure to Part 2 and used to locate defective components within the malfunctioning circuits.

6.2 TROUBLESHOOTING TECHNIQUES FOR INDIVIDUAL COMPONENTS

6.2.1 Bipolar Transistor

1. A transistor is defective if more than one volt (typically 0.7V) across the base/emitter junction is measured in the forward direction.
2. A transistor, when used as a switch, may have a few volts reverse bias voltage.

6.2.2 Diode

A diode is defective if it has greater than one volt (typically 0.7V) forward voltage across it (except Zener and LED).

6.2.3 Operational Amplifier (e.g., 741, CA3030)

The + and — inputs of an operational amplifier should have less than 15 mV difference when operating under normal conditions.

6.2.4 FET (Field Effect Transistor)

1. No gate current should be drawn by the gate. If so, the FET is defective.
2. The gate-to-source voltage is always reversed biased under normal operating conditions. If otherwise, the FET is defective.

6.2.5 Capacitor

1. Shorted capacitors have zero volts across their terminals.
2. Opened capacitor can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.

6.3 QUICK TROUBLESHOOTING GUIDE

Symptom	Corrective Action
Blown Line Fuse	Replace fuse. If it blows again, check the following: 1. One of the four transistors mounted on the rear panel is shorted to itself or to chassis ground. 2. Bypass capacitors for power supply are shorted. 3. Follow algorithm (Figure 6-1) to locate short in a particular supply.

Symptom	Corrective Action
+15V Power Supply Malfunction	1. Voltage low: a. Transformer output low. b. Extra current loading; check for overheated and defective component. Use P1, P2 and P3 for isolation of current loading. 2. Voltage high: a. Power transistor Q1 and Q2 shorted. b. IC1 defective.
Other Power Supply Malfunctions	1. Use similar procedure for troubleshooting as in the +15V power supply malfunctions. 2. Follow Figure 6-1 to locate problem in a particular power supply.
No Output Signals	1. If no ∿ signal is present at output of integrator, follow Figure 6-2 for trouble-shooting. 2. If no signal is present at TP5, check function selector in Table 6-1. 3. If no signal is seen at junction of R243 and R245, follow Figure 6-3, output amplifier.
∿ but no ∿ , ⎍ or ⌐	Follow Table 6-1 to check out the corresponding circuit.
Frequency Accuracy Out of Specification	1. Check frequency calibration. 2. Check for frequency change when changing frequency bit-by-bit; if problem appears to be in frequency setting, check D/A circuitry.
Amplitude Accuracy Out of Specification	1. Check calibration. 2. Check for amplitude change when changing amplitude bit-by-bit; if problem appears to be in amplitude setting, check D/A circuitry. 3. Check for saturation of output amplifier (50Ω loaded; amplitude plus dc offset should not exceed 10V p-p).
DC Offset Accuracy Out of Specification	1. Check calibration. 2. Check for offset change when changing offset bit-by-bit; if problem appears to be in offset setting, check D/A circuitry.
TRIG and GATED Mode Inoperative	1. Check for correct signals in the trigger circuit using Table 6-1.

Table 6-1. KEY SIGNALS, VOLTAGES AND STATES AT THE ANALOG BOARD

Frequency Range Logic

FR2	FR1	FR0	IC6 Pin In Low State	Frequency Range (Ex = X 10^X)
L	L	L	10	E0
L	L	H	11	E1
L	H	L	12	E2
L	H	H	13	E3
H	L	L	4	E4
H	L	H	3	E5
H	H	L	2	E6
H	H	H	1	E7

Generator Enable Circuit (Analog Board)

	Continuous	Trig/Gated (No Ext Trigger)
1. P3 pin 31 (OPERATE)	Low State	High State
2. Q14 base	0V	≈ 0.7V

Integrator

1. IC9 pin 4	≈ 0V
2. IC9 pin 5	≈ 1.4V
3. IC11 pin 12	≈ 2.5V p-p ∿
4. R135 & R136 junction	2.5V p-p ∿

Comparator Switch

1. Q2 & Q6 emitters	≈ +9V
2. IC7 pins 2 & 8	≈ −1V
3. Q2 base	≈ +8V with 0.5V p-p ⎍
4. Q6 base	≈ +8V with 0.5V p-p ⎍ opposite phase of Q2 base
5. Q1 emitter	≈ +2V/−1.5V ⎍
6. Q7 emitter	≈ +2V/−2.5V ⎍

Ramp Amplifier

1. Q8 & Q12 emitters	+0.7V/−2V ⎍
2. IC8 pin 1	≈ +11V
3. IC8 pins 3 & 11	≈ −3V with ≈ 0.5V p-p ⎍ opposite phase from pin 3 to pin 11
4. IC8 pin 6	+1.25V
5. IC8 pin 2	2.5V p-p ∿
6. Q9 emitter	2.5V p-p ⌝

VCG

Voltages depend upon frequency setting.

1. P3 pin 46 (D/F)	0 to −10V
2. IC1 pin 6	0 to +3.7V
3. Q3 emitter	−0.7V to −4.0V
4. IC3 pin 6	+0.7V to +4.0V

Sine Converter and Amplifier

1. IC12 pin 6	≈ 1.2 mV p-p ∿
2. IC10 pin 4	≈ 250 mV p-p ∿
3. IC10 pin 12	2.5V p-p ∿

Function Selector

$\overline{F0}$	$\overline{F1}$	Function	Collector of Q43	Q18	Q19	Q20
H	H	∿	≈ +5V	≈ −14V	≈ −14V	≈ −14V
H	L	∿	≈ −14V	≈ +5V	≈ −14V	≈ −14V
L	H	⎍	≈ −14V	≈ −14V	≈ +5V	≈ −14V
L	L	⌐	≈ −14V	≈ −14V	≈ −14V	≈ +5V

X-Y Multiplier, Inverting Amplifier and Output Amplifier

1. P3 pin 7 (D/V)	−2V to +2V depending on amplitude setting and polarity
2. IC17 pin 4	Selected ∿ , ∿ , ⎍ or ⌝
3. IC17 pins 3 & 13	≈ −13V
4. IC17 pin 1	≈ 6V
5. IC17 pins 2 & 14	≈ 11V with low level amplitude of selected function
6. Q27 emitter	≈ −4V
7. Q21 base	≈ +13V
8. Q22 base	≈ −13V
9. Q28 emitter	≈ +6V
10. Q32 emitter	≈ +6V
11. Q33 base	≈ +13V
12. Q34 base	≈ −13V
13. Q37 & Q38 collectors	≈ twice programmed amplitude p-p
14. R243 & R245 junction	≈ twice programmed amplitude p-p
15. Q21, Q22, Q27 thru Q38, Q41 & Q42	On in any normal state (i.e., base/emitter drop should be ≈ 0.7V in forward bias direction)
16. Q39 & Q40	On only when output sinks or sources >100 mA

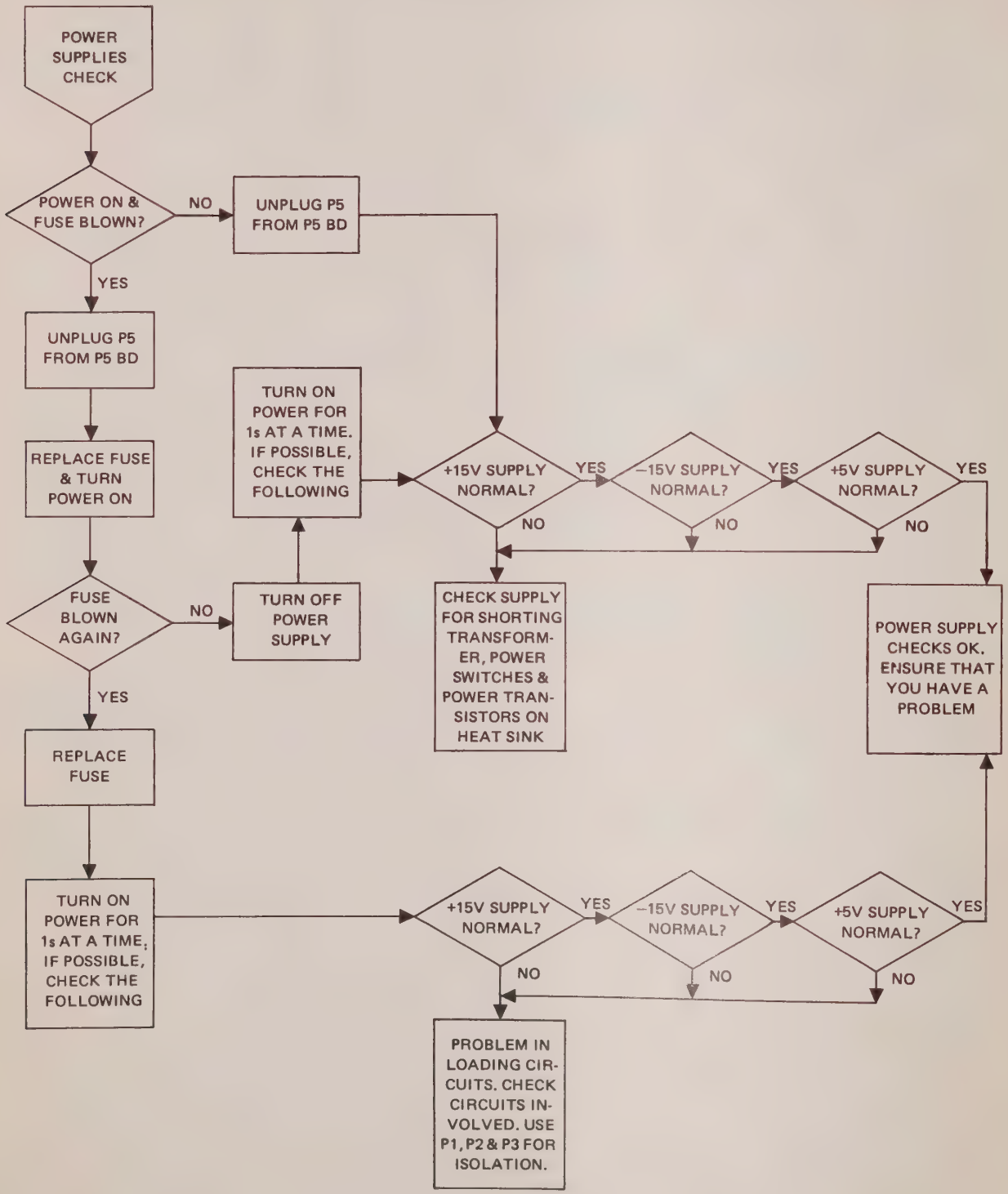


Figure 6-1. Power Supply Algorithm

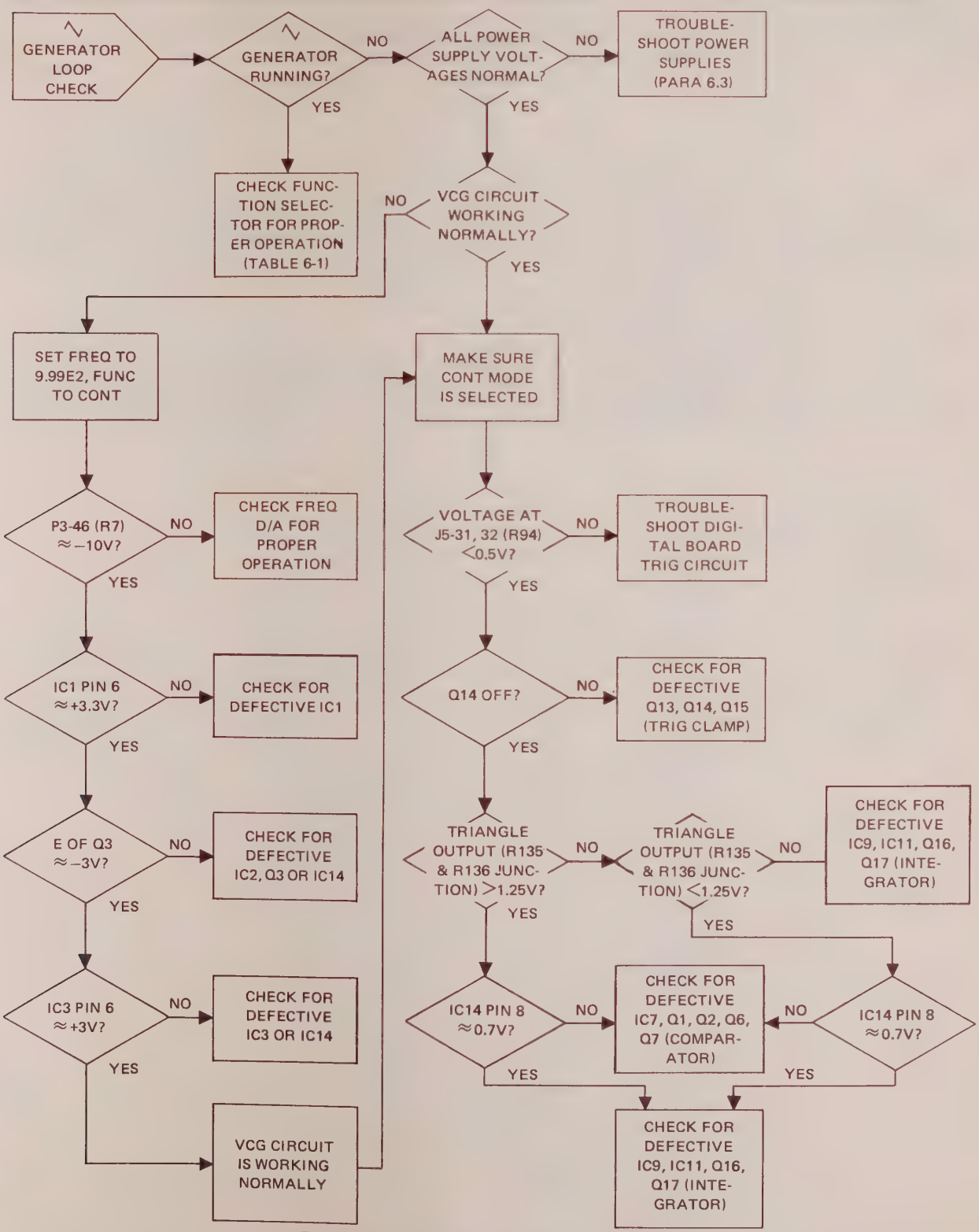


Figure 6-2. Integrator, Comparator and VCG Algorithm

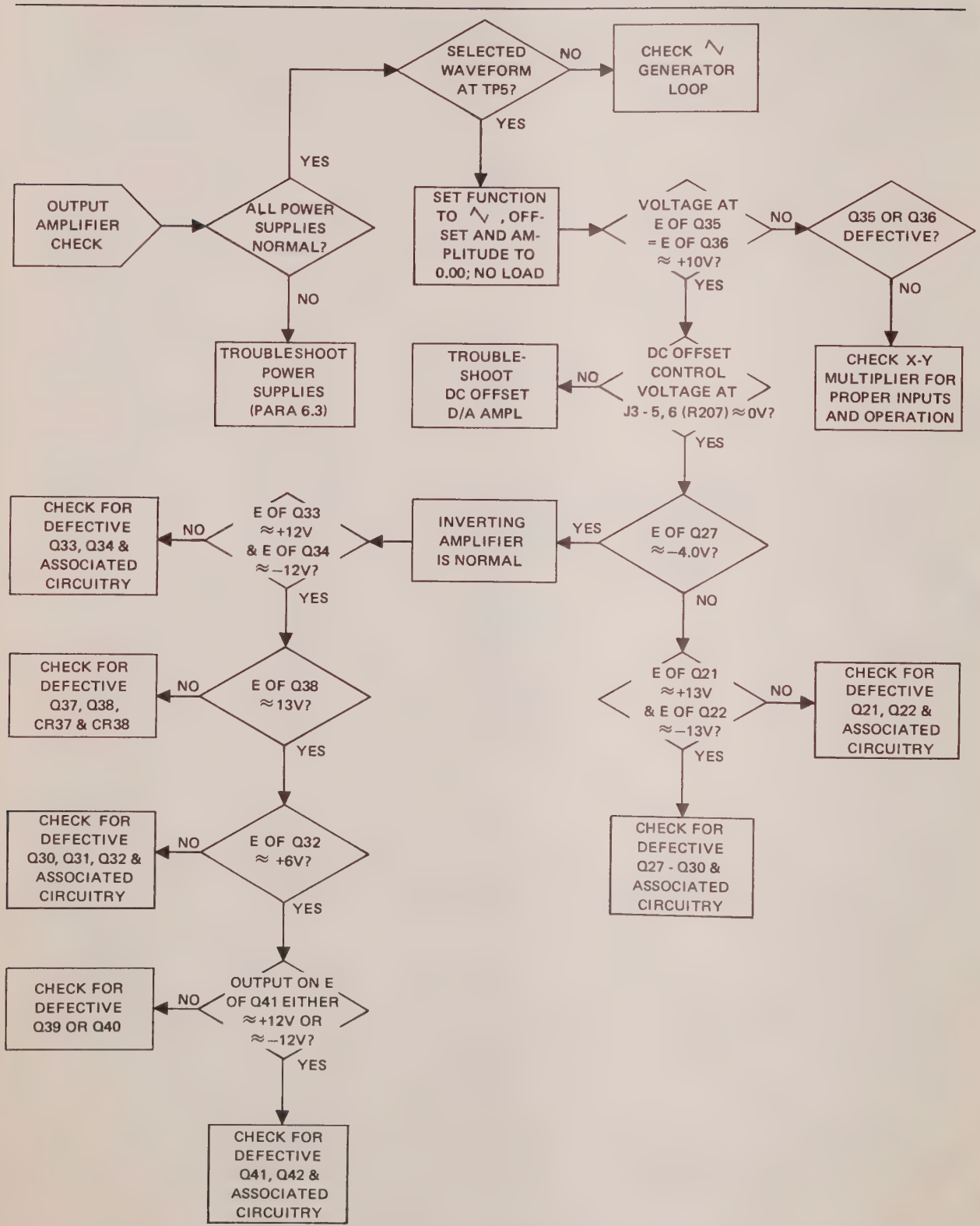

OUTPUT AMPLIFIER CHECK
ALL POWER SUPPLIES NORMAL?
NO
TROUBLESHOOT POWER SUPPLIES (PARA 6.3)
YES
SELECTED WAVEFORM AT TP5?
NO
CHECK ∿ GENERATOR LOOP
YES
SET FUNCTION TO ∿, OFFSET AND AMPLITUDE TO 0.00; NO LOAD
VOLTAGE AT E OF Q35 = E OF Q36 ≈ +10V?
NO
Q35 OR Q36 DEFECTIVE?
NO
CHECK X-Y MULTIPLIER FOR PROPER INPUTS AND OPERATION
YES
DC OFFSET CONTROL VOLTAGE AT J3 - 5, 6 (R207) ≈ 0V?
NO
TROUBLESHOOT DC OFFSET D/A AMPL
YES
E OF Q27 ≈ −4.0V?
YES
INVERTING AMPLIFIER IS NORMAL
NO
E OF Q21 ≈ +13V & E OF Q22 ≈ −13V?
NO
CHECK FOR DEFECTIVE Q21, Q22 & ASSOCIATED CIRCUITRY
YES
CHECK FOR DEFECTIVE Q27 - Q30 & ASSOCIATED CIRCUITRY
E OF Q33 ≈ +12V & E OF Q34 ≈ −12V?
NO
CHECK FOR DEFECTIVE Q33, Q34 & ASSOCIATED CIRCUITRY
YES
E OF Q38 ≈ 13V?
NO
CHECK FOR DEFECTIVE Q37, Q38, CR37 & CR38
YES
E OF Q32 ≈ +6V?
NO
CHECK FOR DEFECTIVE Q30, Q31, Q32 & ASSOCIATED CIRCUITRY
YES
OUTPUT ON E OF Q41 EITHER ≈ +12V OR ≈ −12V?
NO
CHECK FOR DEFECTIVE Q39 OR Q40
YES
CHECK FOR DEFECTIVE Q41, Q42 & ASSOCIATED CIRCUITRY

Figure 6-3. Output Amplifier Algorithm

SECTION 7
PARTS LISTS AND SCHEMATIC DIAGRAMS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

7.2 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit, and if applicable, the function performed.

7.3 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

Drawings	Old Number	New Number
Instrument Schematic	158-200	0004-00-0045
Chassis Assembly	159-000	0102-00-0304
Chassis Parts List	159-000	1101-00-0045
Digital Board Schematic	158-218	0103-00-0106
Digital Board Assembly	158-018	0101-00-0106
Digital Board Parts List	158-018	1101-00-0106
Analog Board Schematic	158-219	0103-00-0107
Analog Board Assembly	158-019	0101-00-0107
Analog Board Parts List	158-019	1101-00-0107
Front Panel Assembly	159-046	0102-00-0333
Front Panel Parts List	159-046	1101-00-0075
Key Board Schematic	158-247	0103-00-0109
Key Board Assembly	158-047	0101-00-0109
Key Board Parts List	158-047	1100-00-0109
Display Board Schematic	158-251	0103-00-0105
Display Board Assembly	158-051	0101-00-0105
Display Board Parts List	158-051	1100-00-0105
Rear Panel Assembly	158-034	0102-00-0332
Rear Panel Parts List	158-034	1100-00-0074
Power Supply Schematic	158-220	0103-00-0108
Power Supply Assembly	158-020	0101-00-0108
Power Supply Parts List	158-020	1100-00-0108
158 Instrument Schematic	158-235	0004-00-0081
158 Modification	158-000	0102-00-0303
158 Modification Parts List	158-000	1101-00-0044
158 Front Panel Assembly	158-038	0102-00-0336
158 Front Panel Parts List	158-038	1101-00-0078
158 Cable Assembly	158-039	1203-00-0005

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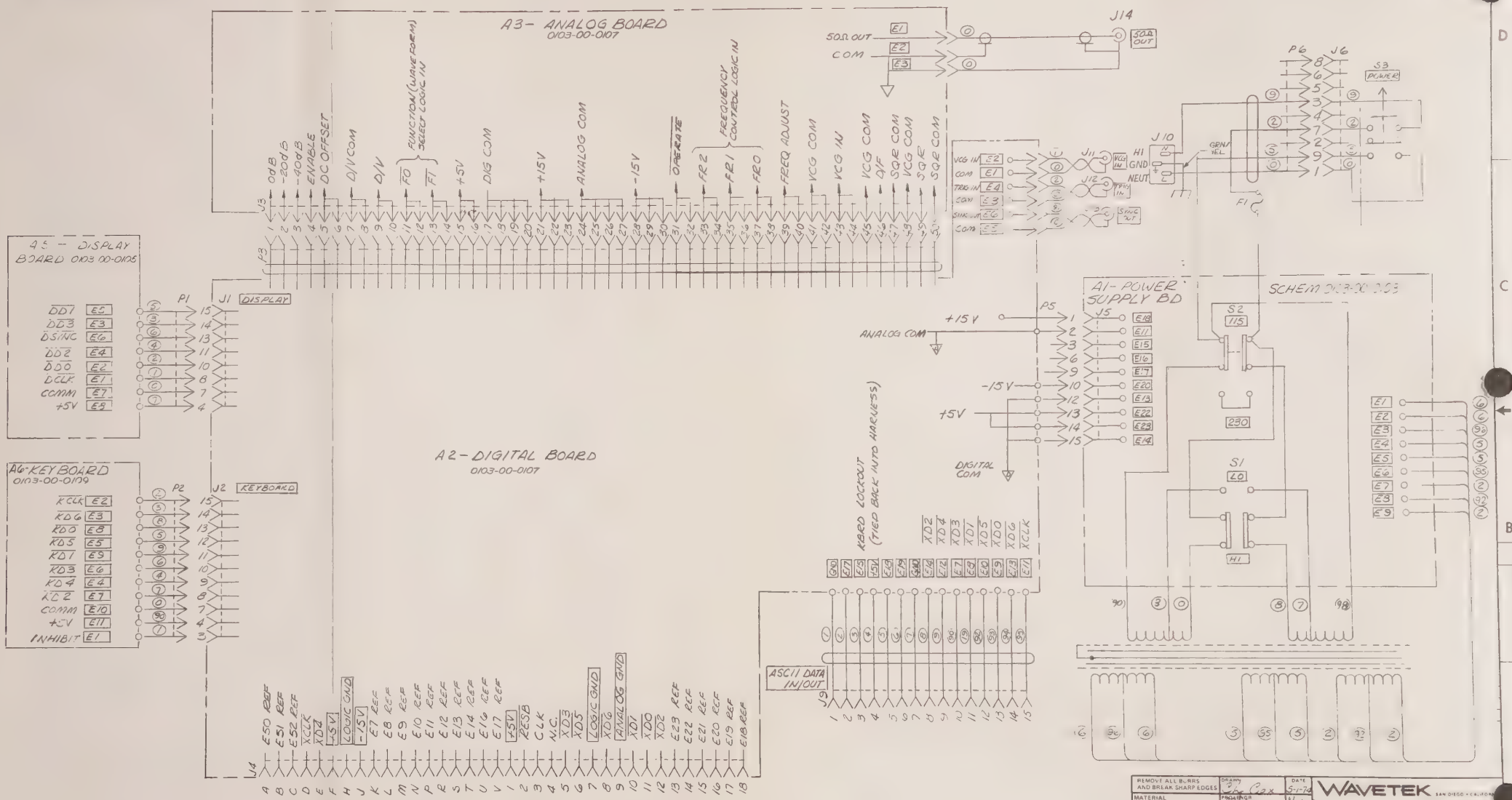
REV	ECN	BY	DATE	APP
A	ECN 1133	[illegible]	[illegible]	[illegible]
B	ECN 1368	PG	11-17-77	AYS
C	# 920	[illegible]	5-1-78	



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN [illegible]	DATE 5-1-78	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	ENGINEER [illegible]	DATE 11/17/77	TITLE	INTERCONNECT DIAGRAM -NO OPTION-
FINISH WAVETEK PROCESS	RELEASE APPROVED [illegible]	DATE 11/30/78		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 010 ANGLES ± 1° XX ± 030		MODEL NO 158/159	DWG NO 0004-00-0045 REV C
	DO NOT SCALE DWG		CODE IDENT 23338	SHEET 1 OF 1
	SCALE			

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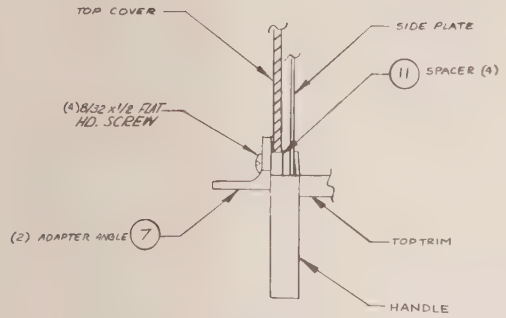
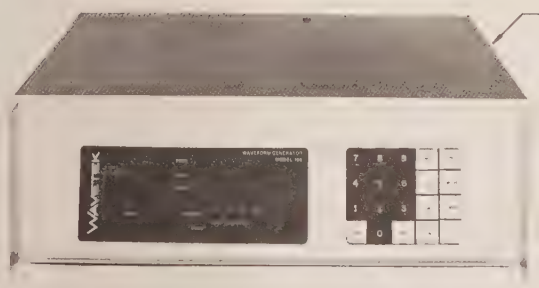
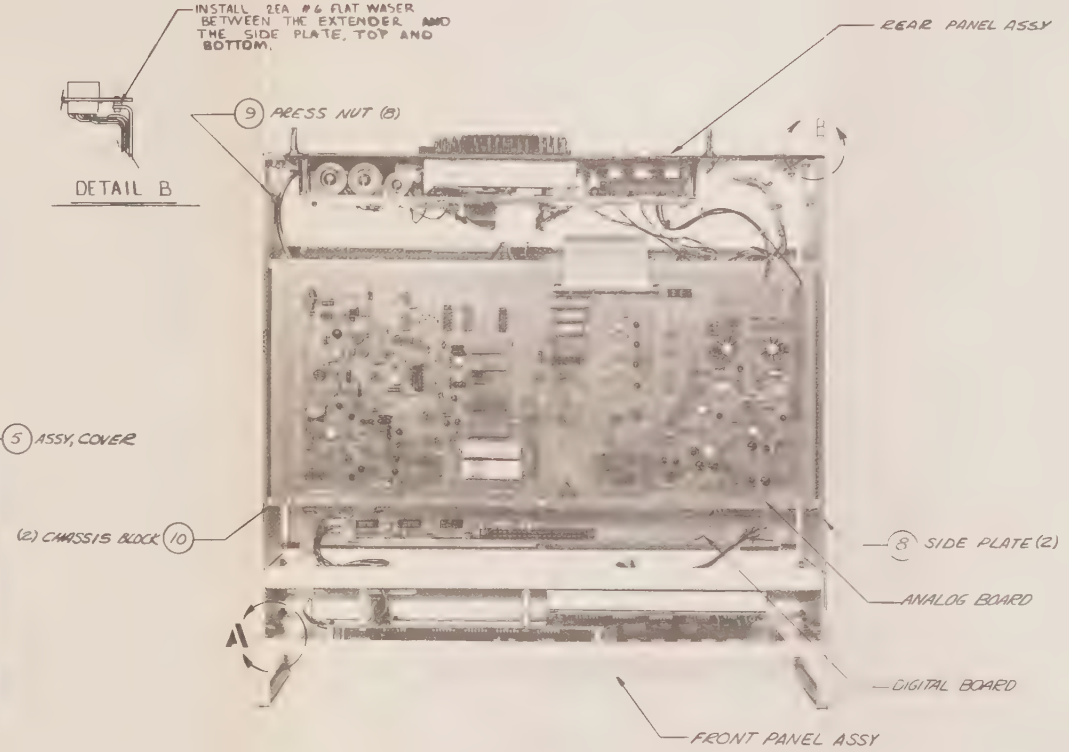
REV	E N	BY	DATE	APP
A	1069	CL	9/10	XPS
B	ECN 1128	CL	3/14	XPS
C	96	KM	1/15	XPS
D	ECN 1754	RO	2/28	



DETAIL A

DETAIL B





TOP VIEW WITH COVERS REMOVED

1. ITEM G#7 ARE NOT SHOWN.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN C.L. Cox	DATE 3/24/78
MATERIAL —	ENGINEER I.P. Palmeri	4/12/78
FINISH WAVETEK PROCESS —	RELEASED APPROV XPS	12/14/78
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX .010 ANGLES ±1 .XX .030	DO NOT SCALE DWG	SCALE NONE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: ASSEMBLY CHASSIS

MODEL NO	DWG NO	REV
159	0102-00-0304	D

CODE IDENT 23338 SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	DWG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, CHASSIS	0102-00-0304	WVTK	0102-00-0304	1
5	COVER ASST	158-045	WVTK	1201-00-0019	1
6	PLATE,SIDE	158-310	WVTK	1400-00-0673	2
7	BRKT,ANGLE,W/A	140-373-PAINT	WVTK	1400-00-2712	2
11	SPACER,W/A	147-362	WVTK	1400-00-5693	4
9	INSERT # 6	74-11-106-13	SOTCO	2800-04-0017	8
10	FAST,CHASSIS	1591-C11	USECO	2800-04-0022	2
NONE	PWR CORD	0-7788-008-GY	PACND	6001-80-0005	1

WAVETEK PARTS LIST	TITLE STU CHASSIS	ASSEMBLY NO 1101-00-0045	REV D
		PAGE: 1	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PRT ENGR		TITLE CHASSIS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 158/159	DWG NO 1101-00-0045 REV L
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

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REV	ECN	BY	DATE	APP
A	ECN 1518	RO	2/4/77	
B	ECN 1754	RO	6-19-78	

OPTIONAL INTERFACE CONVERSION PCA

OPTIONS ONLY — OPTIONS ONLY — -15V — ANALOG COMM — +5V — DIG COMM — OPTIONS ONLY — XCLK (OPT OUT) — XD6 (OPT OUT) — XD5 (OPT OUT) — XD4 (OPT OUT) — XD3 (OPT OUT) — XD1 (OPT OUT) — XD7 (OPT OUT) — XD2 (OPT OUT)

U V 18 17 T R K L N M S P 2 3 4 16 15 14 13 J 9 1 7 H F C B A D B 11 6 10 5 E 12

INTERFACE CONNECTOR J4

J5

1	(1)	E16	
2	(2)	E17	
3	(3)	E15	
+5V 4	(4)	+5V	+5V
5	(5)	E18	
6	(6)	E19	
GND 7	(7)	GND	
8	(8)	E14	
9	(9)	E12	
10	(91)	E7	
11	(92)	E8	
12	(93)	E10	
13	(94)	E9	
14	(95)	E13	
15		E11	

(28T) E25B — (34T) E2E — N.C. — E20 E21 E22 E23 — -15V — +5V — +5V — E52 E51 E50

STANDARD INTERFACE ENABLE STRAPS (REMOVED IN OPTIONS)

E45	XD2	E43	
E35	XD4	E44	
E33	XD3	E34	
E37	XD1	E36	
E41	XD5	E40	
E39	XD0	E38	
E47	XD6	E46	
E43	XCLK	E42	

KEYBOARD J2

N.C.	1
N.C.	2
KEYBOARD INHIBIT	3
+5V	4
N.C.	5
N.C.	6
COM	7
XD2	8
XD4	9
XD3	10
XD1	11
XD5	12
XD0	13
XD6	14
XCLK	15

CONTROL	ASCII	D6	D5	D4	D3	D2	D1	D0
CNS	_	L	H	H	H	H	L	H
0	0	L	H	H	L	L	L	L
1	1	L	H	H	L	L	L	H
2	2	L	H	H	L	L	H	L
3	3	L	H	H	L	L	H	H
4	4	L	H	H	L	H	L	L
5	5	L	H	H	L	H	L	H
6	6	L	H	H	L	H	H	L
7	7	L	H	H	L	H	H	H
8	8	L	H	H	H	L	L	L
9	9	L	H	H	H	L	L	H
AMPL	A	H	L	L	L	L	L	H
MODE	B	H	L	L	L	L	H	L
FUNC	C	H	L	L	L	L	H	H
SPST	D	H	L	L	L	H	L	L
MULT	E	H	L	L	L	H	L	H
MULT (NOTE)	SP	L		L	L	L	L	L
FREQ	F	H	L	L	L	H	H	L
UNIT	G	H	L	L	L	H	H	H
ON	H	H	L	L	H	L	L	L
OFF	I	H	L	L	H	L	L	H

NOTE: USE OF ASCII SPACE (SP) ENABLED ONLY BY AN IMMEDIATELY PRECEDING IMMEDIATE

OPERATION	CONTROLS
CONT	MODE 0
TRIG	MODE 1
GATE	MODE 2
∿	FUNC 0
⋀	FUNC 1
⎍	FUNC 2
⎍	FUNC 3

CLK =	$\overline{KCLK}$ OR $\overline{XCLK}$
D0 =	$\overline{KD0}$ OR $\overline{XD0}$
D1 =	$\overline{KD1}$ OR $\overline{XD1}$
D2 =	$\overline{KD2}$ OR $\overline{XD2}$
D3 =	$\overline{KD3}$ OR $\overline{XD3}$
D4 =	$\overline{KD4}$ OR $\overline{XD4}$
D5 =	$\overline{KD5}$ OR $\overline{XD5}$
D6 =	$\overline{KD6}$ OR $\overline{XD6}$
DATA BIT	(KEYBOARD) FROM J2 — (REMOTE) FROM J7

IC42 B — D2 (2D8, 2B8) — IC34 D — D4 (2C8) — IC42 C — D3 (2C8, 2B8) IC42 D — D1 (2C8, 2D8, 2D2) — D5 (2C8) IC34 B — IC42 A — D0 (2D8, 2C8, 2D2, 2B5) — IC34 C — D6 (2C8) — IC34 A — CLK (2C8)

TERMINATION SOCKET XIC41 — +5V — 14

IC 41 TERMINATION PACK (ONE PER MULTI-UNIT GROUP)

+5V — 220Ω — (C) (G) (L) (A) (J) (Q) (E) (N)

8 3 9 5 1 6 4 2 7

330Ω — (D) (H) (M) (B) (K) (R) (F) (P)

5 CONNECTOR FOR "ASCII DATA IN/OUT" OR "ISOLATED ASCII DATA IN" FOR APPROPRIATE PIN ASSIGNMENT SEE INTERCONNECT DIAGRAM.

4 BAR OVER MNEMONIC DENOTES TRUE-WHEN-LOW.

3. ○ DENOTES WIRE COLOR PER RESISTOR CODE.

2. ▭ DENOTES ACTUAL LABELING ON BOARD.

1. ⊐▷* DENOTES OPEN COLLECTOR.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES — WATER A.L. — FINISH WAVETEK PROCESS — DRAWN L. Cox 9/15/76 — ENGINEER — RELEASE APPROV — 4/6/77 — TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030 — DO NOT SCALE DWG — SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC A2 DIGITAL BOARD INTERFACE BUS)

MODEL NO 158/159 — DWG NO 0103-00-0106 — REV B — CODE IDENT 23338 — SHEET 1 OF 6

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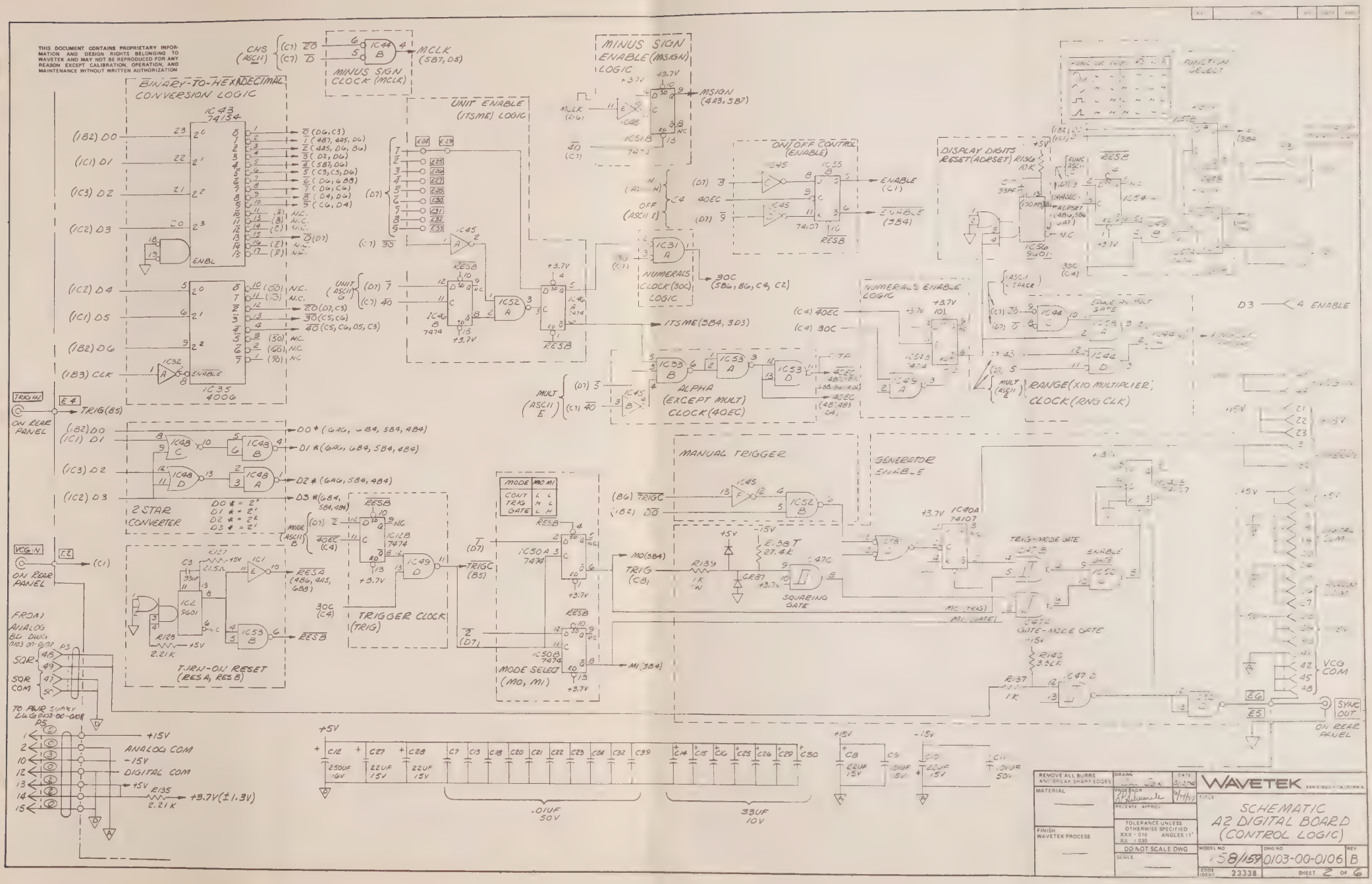

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE 5/24	WAVETEK SAN DIEGO, CA.
MATERIAL	PROJ. ENGR.	RELEASE APPROV.	TITLE: SCHEMATIC A2 DIGITAL BOARD (CONTROL LOGIC)
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1° XX ± .030	DO NOT SCALE DWG	MODEL NO. 158/159 DWG NO. 0103-00-0106 REV. B
	SCALE		CODE IDENT. 23338 SHEET 2 OF 6

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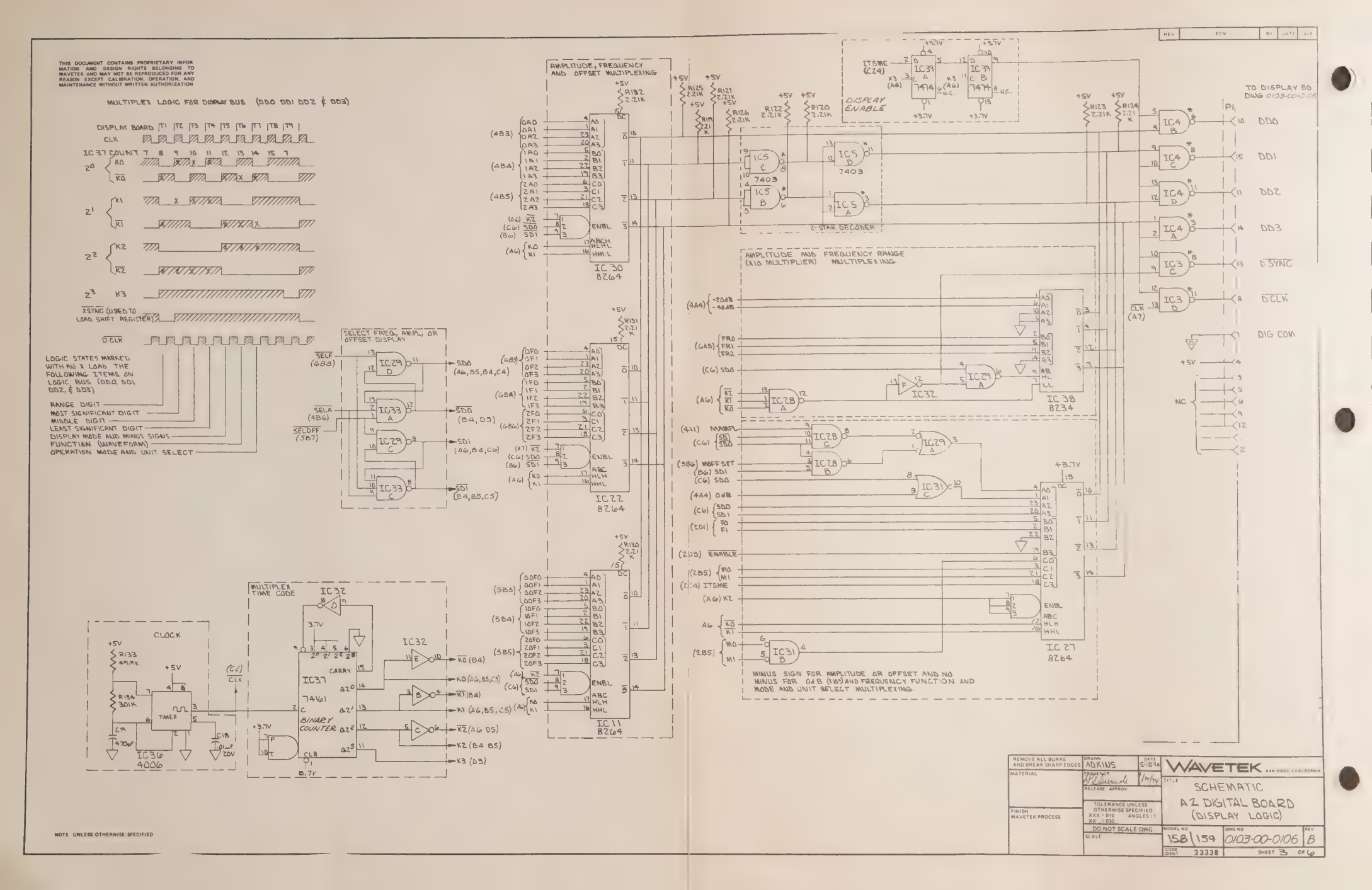

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN ADKINS	DATE 5-28-74	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	ENGINEER		TITLE SCHEMATIC A2 DIGITAL BOARD (DISPLAY LOGIC)
	RELEASE APPROV	8/14/74	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 158 / 159 DWG NO 0103-00-0106 REV B
	SCALE		CODE IDENT 23338 SHEET 3 OF 6

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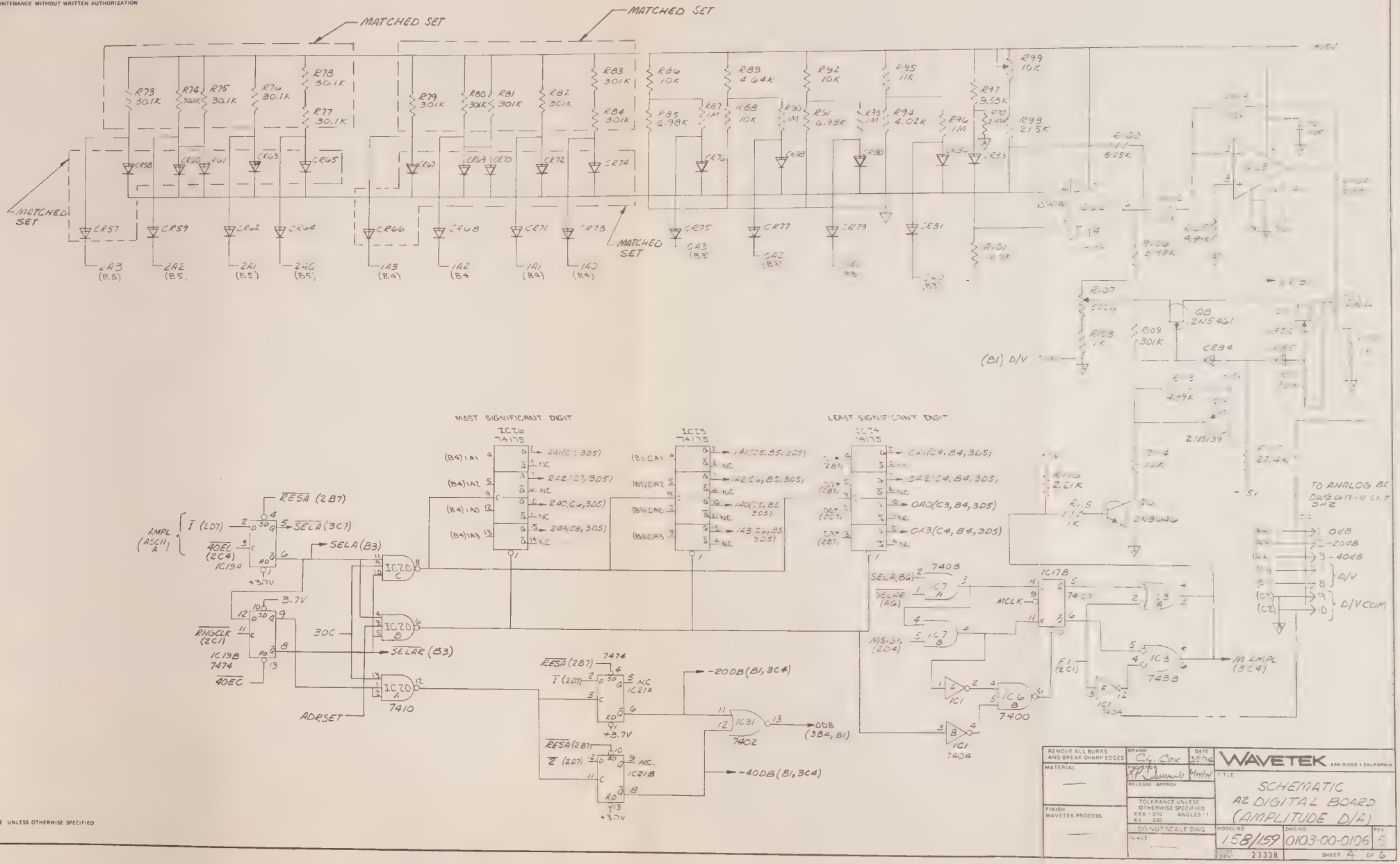

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN C.G. Cox	DATE 3/8/74	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	APPROVED	6/11/74	TITLE SCHEMATIC A2 DIGITAL BOARD (AMPLITUDE D/A)
FINISH WAVETEK PROCESS —	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		MODEL NO 158/159
	DO NOT SCALE DWG		DRG NO 0103-00-0106 REV E
	SCALE —		CAGE CODE 23338 SHEET 4 OF 6

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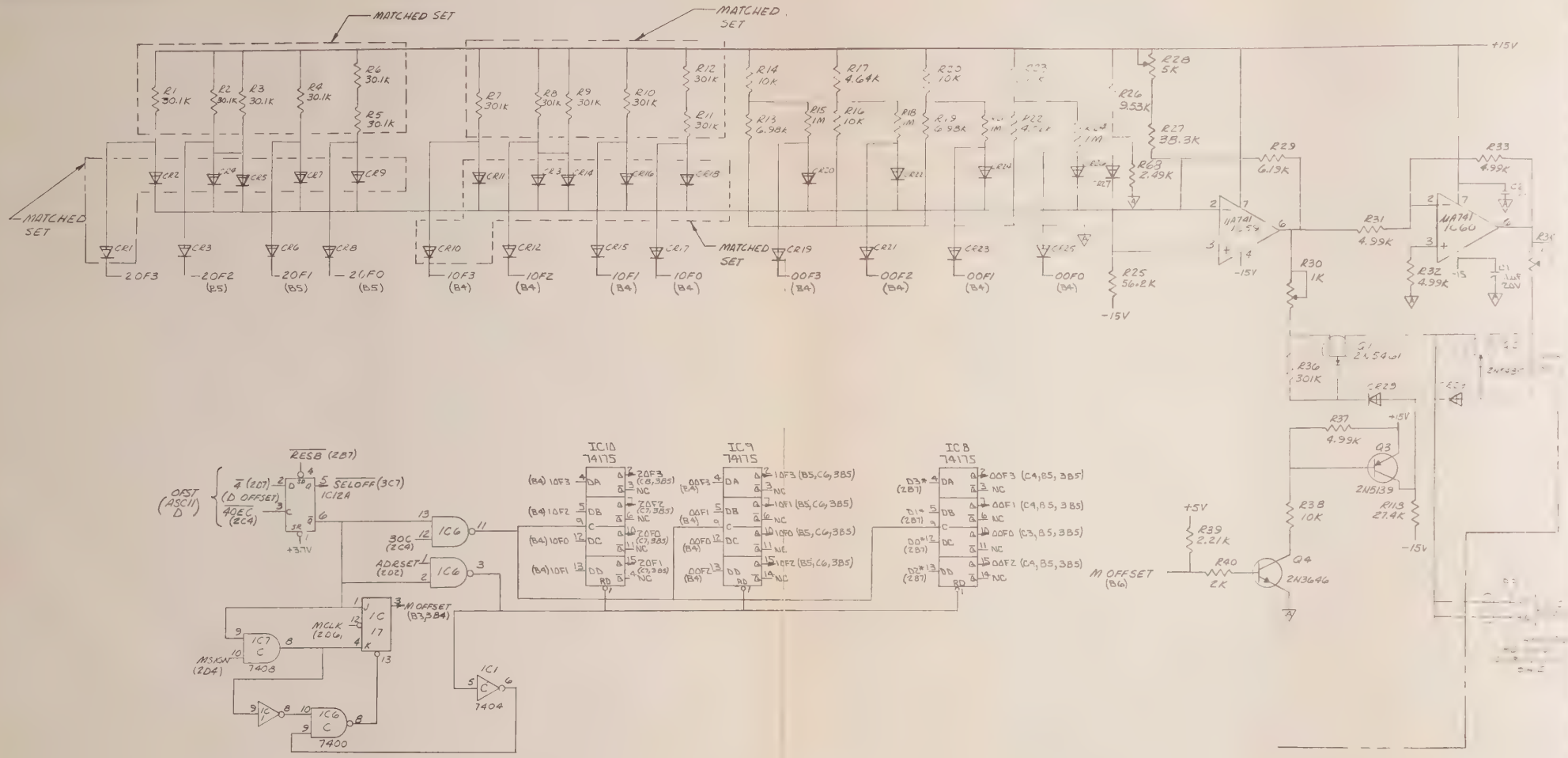

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN C.L. Cox	DATE 3/4/74
MATERIAL —	PROGRAMER F.P. Edwards	3/4/74
FINISH WAVETEK PROCESS —	RELEASE APPROV	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030	
	DO NOT SCALE DWG	
	SCALE —	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC A2 DIGITAL BOARD (OFFSET D/A)

MODEL NO 158/159 | DWG NO 0103-00-0106 | REV B

CODE IDENT 23338 | SHEET 5 OF 6

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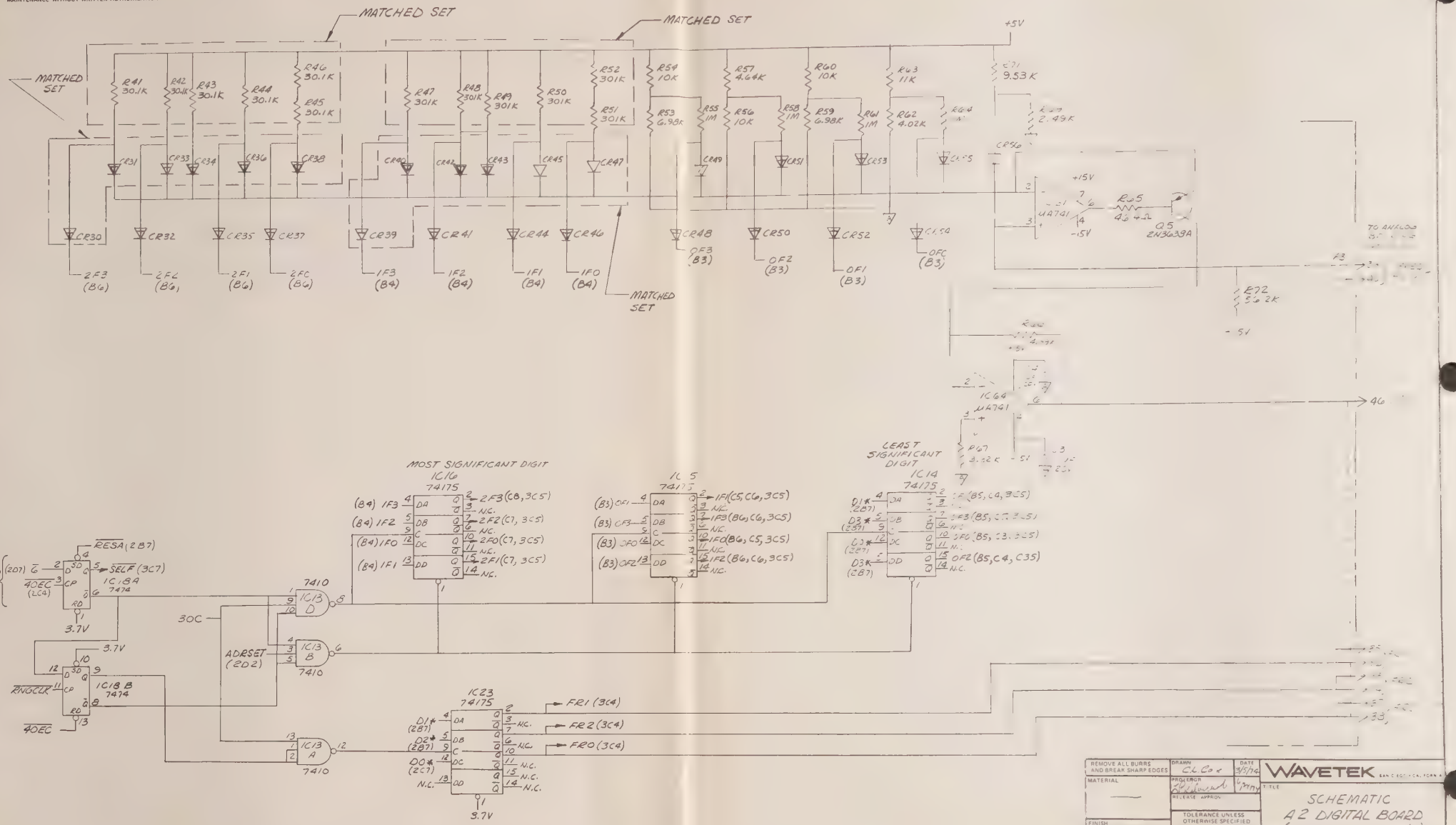

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN C.L. Cox	DATE 3/5/76	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROG ERR		TITLE SCHEMATIC A2 DIGITAL BOARD (FREQUENCY D/A)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ±1°		
	DO NOT SCALE DWG		MODEL NO 158/1159 DWG NO 0103-00-0106 REV B
	SCALE		CODE IDENT 23338 SHEET 6 OF 6

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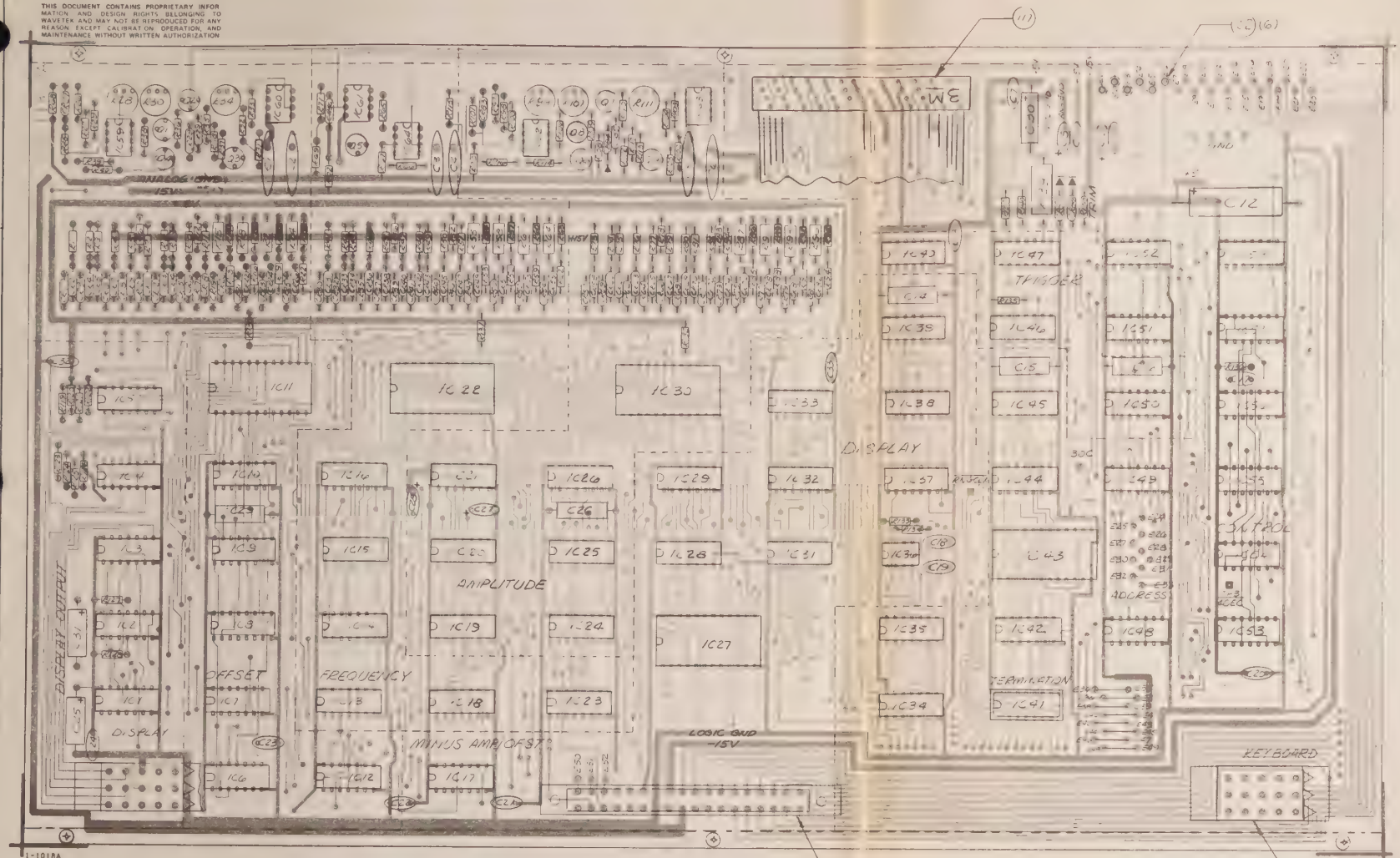
REV	ECN	BY	DATE	APP
A	ECN 1562			
B	ECN 1754	RD		



(16)

(119) (3)
(150)

(135) SUPPORT BAR (2)

1. ALL DIODES ARE POSITIONED AS SHOWN

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN C.L. Cox	DATE 3/29/78	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	ENGINEER	DATE 6/11/15	TITLE ASSEMBLY DIGITAL BOARD
FINISH WAVETEK PROCESS	REVIEW	DATE 6/24/15	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1° XX .030		
	DO NOT SCALE DWG	MODEL NO 158/159	DWG NO 0101-00-0106 REV B
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 1

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REV	E.N.	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DWG, DIGITAL	0101-00-0106	WVTK	0101-00-0106	1
NONE	SCHEMATIC, DIGITAL	0103-00-0106	WVTK	0103-00-0106	1
NONE	CABLE ASSY	158-400	WVTK	1207-00-0003	1
135	BAR,SUPPORT	158-312	WVTK	1400-00-0683	2
C11 C13 C18 C20 C21 C22 C23 C24 C32 C33 C7 C9	CAP,CER,.01MF,50V	CK-103	CRL	1500-01-0310	12
C1 C2 C3 C4 C5 C6	CAP,CER,.1MF,20V	UK20-104	ARCO	1500-01-0413	6
C17	CAP,CER,33PF,1KV	DD-330	CRL	1500-03-3011	1
C19	CAP,CER,470PF,1KV	DD-471	CRL	1500-04-7111	1
C12	CAP,ELECT,250MF,16V	S00D257G016DF7	SPRAG	1500-32-5101	1
C10 C27 C28 C8	CAP,TANT,22MF,15V	196D226X9015KA1	SPRAG	1500-72-2601	4
C14 C15 C16 C25 C26 C29 C30 C31	CAP,TANT,33MF,10V	150D336X9010B2	SPRAG	1500-73-3601	8
NONE	DIGITAL	158-118	WVTK	1700-00-0106	1
119	CONN,15PIN	03-09-1151	MOLEX	2100-02-0012	3
NONE	PLUG,15PIN	03-09-2151	MOLEX	2100-02-0013	1
134	SKT,IC,14PIN	14-DIP	CINCH	2100-03-0011	1
110	CONN,EDGE CARD	252-18-30-160	CINCH	2100-03-0013	1

WAVETEK PARTS LIST | TITLE DIGITAL | ASSEMBLY NO 1100-00-0106 | PAGE: 1 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R116 R119 R120 R121 R122 R123 R124 R125 R126 R128 R130 R131 R132 R135 R39	RES,MF,1/8W,1%,2.21K	RN55D-2211F	TRW	4701-03-2211	15
R68 R69 R70	RES,MF,1/8W,1%,2.49K	RN55D-2491F	TRW	4701-03-2491	3
R117 R118 R138T	RES,MF,1/8W,1%,27.4K	RN55D-2742F	TRW	4701-03-2742	3
R109 R110 R134 R35 R36	RES,MF,1/8W,1%,301K	RN55D-3013F	TRW	4701-03-3013	5
R140 R67	RES,MF,1/8W,1%,3.32K	RN55D-3321F	TRW	4701-03-3321	2
R104 R106	RES,MF,1/8W,1%,3.83K	RN55D-3831F	TRW	4701-03-3831	2
R27	RES,MF,1/8W,1%,38.3K	RN55D-3832F	TRW	4701-03-3832	1
R100 R22 R62 R94	RES,MF,1/8W,1%,4.02K	RN55D-4021F	TRW	4701-03-4021	4
R17 R57 R89	RES,MF,1/8W,1%,4.64K	RN55D-4641F	TRW	4701-03-4641	3
R65	RES,MF,1/8W,1%,46.4	RN55D-46R4F	TRW	4701-03-4649	1
R105 R113 R31 R32 R33 R37 R66	RES,MF,1/8W,1%,4.99K	RN55D-4991F	TRW	4701-03-4991	7
R133	RES,MF,1/8W,1%,49.9K	RN55D-4992F	TRW	4701-03-4992	1
R101 R25 R72	RES,MF,1/8W,1%,56.2K	RN55D-5622F	TRW	4701-03-5622	3
R29	RES,MF,1/8W,1%,6.19K	RN55D-6191F	TRW	4701-03-6191	1
R13 R14 R53 R59 R85	RES,MF,1/8W,1%,6.98K	RN55D-6981F	TRW	4701-03-6981	5

WAVETEK PARTS LIST | TITLE DIGITAL | ASSEMBLY NO 1100-00-0106 | PAGE: 3 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR14 CR16 CR18 CR2 CR30 CR31 CR33 CR34 CR36 CR38 CR39 CR4 CR40 CR42 CR43 CR45 CR47 CR5 CR57 CR58 CR60 CR61 CR63 CR65 CR66 CR67 CR69 CR7 CR70 CR72 CR74 CR9	QTY:6:4807-02-0000				
Q5	TRANS	2N3638A	FAIR	4901-03-6381	1
Q4 Q6	TRANS	2N3640	FAIR	4901-03-6460	2
Q3 Q9	TRANS	2N5139	FAIR	4901-05-1390	2
Q1 Q8	TRANS	2N5461	MOT	4901-05-4610	2
Q2	TRANS	2N5485	NSC	4901-05-4850	1
Q7	TRANS	NF-510	NSC	4902-00-5100	1
IC36	IC	NE555V	SIG	7000-05-5500	1
IC59 IC60 IC61 IC62 IC63 IC64	IC	MA-741	FAIR	7000-07-4100	6
IC35	IC	4006	MOT	8000-40-0600	1
IC29 IC49 IC6	IC	7400	TI	8000-74-0000	3
IC31 IC44 IC48	IC	7402	TI	8000-74-0200	3
IC5	IC	7403	TI	8000-74-0300	1
IC1 IC32 IC45	IC	7404	TI	8000-74-0400	3

WAVETEK PARTS LIST | TITLE DIGITAL | ASSEMBLY NO 1100-00-0106 | PAGE: 5 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
150	PIN,FEMALE	02-09-1133	MOLEX	2100-05-0004	30
151	PIN,MALE	02-09-2118	MOLEX	2100-05-0005	7
152	PIN,MALE	61182-2	AMP	2100-05-0020	6
153	PIN,FEMALE	02-09-1118	MOLEX	2100-05-0026	14
NONE	TRANSFAD	10123N	METRS	2800-11-0003	1
R30 R34	POT,TRIM,1K	91AM1K	BECK	4600-01-0209	2
R99	POT,TRIM,10K	91AR10K	BECK	4600-01-0315	1
R107 R111	POT,TRIM,500	91AM500	BECK	4600-05-0104	2
R28	POT,TRIM,5K	91AM5K	BECK	4600-05-0205	1
R139	RES,C,1W,10%,1K	MC326F-102	STKPL	4700-35-1001	1
R137	RES,MF,1/8W,1%,100	RN55D-1000F	TRW	4701-03-1000	1
R108 R112 R115	RES,MF,1/8W,1%,1K	RN55D-1001F	TRW	4701-03-1001	3
R102 R103 R114 R136 R16 R18 R20 R38 R54 R56 R60 R86 R88 R92	RES,MF,1/8W,1%,10K	RN55D-1002F	TRW	4701-03-1002	14
R23 R63 R95	RES,MF,1/8W,1%,11K	RN55D-1102F	TRW	4701-03-1102	3
R40	RES,MF,1/8W,1%,2K	RN55D-2001F	TRW	4701-03-2001	1
R127 R96	RES,MF,1/8W,1%,21.5K	RN55D-2152F	TRW	4701-03-2152	2

WAVETEK PARTS LIST | TITLE DIGITAL | ASSEMBLY NO 1100-00-0106 | PAGE: 2 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R41					
R26 R71 R97	RES,MF,1/8W,1%,9.53K	RN55D-9531F	TRW	4701-03-9531	3
R15 R18 R21 R24 R55 R58 R61 R64 R87 R90 R93 R96	RES,MF,1/4W,1%,1M	RN60D-1004F	TRW	4701-13-1004	12
IC41	RES MODULE	899-5-R220/330	BECK	4770-00-0004	1
R1 R2 R3 R4 R41 R42 R43 R44 R45 R46 R5 R6 R73 R74 R75 R76 R77 R78	RES,SET,6-30,1%,1/8W QTY:6:4701-03-3012	158-501-94A	MVTK	4789-00-0025	3
R10 R11 R12 R47 R48 R49 R50 R51 R52 R7 R79 R8 R80 R81 R82 R83 R84 R9	RES,SET,6-301K,1/8W QTY:6:4701-03-3013	157-501-26A	MVTK	4789-00-0030	5
CR12 CR15 CR17 CR19 CR20 CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR28 CR29 CR3 CR32 CR35 CR37 CR41 CR44 CR46 CR48 CR49 CR50 CR51 CR52 CR53 CR54 CR55 CR56 CR59 CR6 CR62 CR64 CR68 CR71 CR73 CR75 CR76 CR77 CR78 CR79 CR8 CR80 CR81 CR82 CR83 CR84 CR85 CR86 CR87	DIODE	FG-6666	FAIR	4807-02-6666	52
CR1 CR10 CR11 CR13	DIODE,SET,6-4.7V-6666	154-500-69	MVTK	4898-04-0001	6

WAVETEK PARTS LIST | TITLE DIGITAL | ASSEMBLY NO 1100-00-0106 | PAGE: 4 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
IC58 IC7	IC	7408	TI	8000-74-0800	2
IC13 IC20 IC28 IC33	IC	7410	TI	8000-74-1000	4
IC52 IC53	IC	7437	TI	8000-74-3700	2
IC3 IC4	IC	7438	TI	8000-74-3800	2
IC12 IC18 IC19 IC21 IC39 IC40 IC55 IC51 IC54 IC57	IC	7474	TI	8000-74-7400	10
IC38	IC	8234	SIG	8000-82-3400	1
IC11 IC22 IC27 IC30	IC	8284	SIG	8000-82-8400	4
IC43	IC	8311/9311	FAIR	8000-83-1100	1
IC2 IC56	IC	8601/9601	FAIR	8000-86-0100	2
IC17 IC40 IC55	IC	74107	TI	8007-41-0700	3
IC34 IC42 IC47	IC	74132	TI	8007-41-3200	3
IC37	IC	74161	TI	8007-41-6100	1
IC10 IC14 IC15 IC16 IC23 IC24 IC25 IC26 IC8 IC9	IC	74175	TI	8007-41-7500	8

WAVETEK PARTS LIST | TITLE DIGITAL | ASSEMBLY NO 1100-00-0106 | PAGE: 6 | REV D

NOTE UNLESS OTHERWISE SPECIFIED

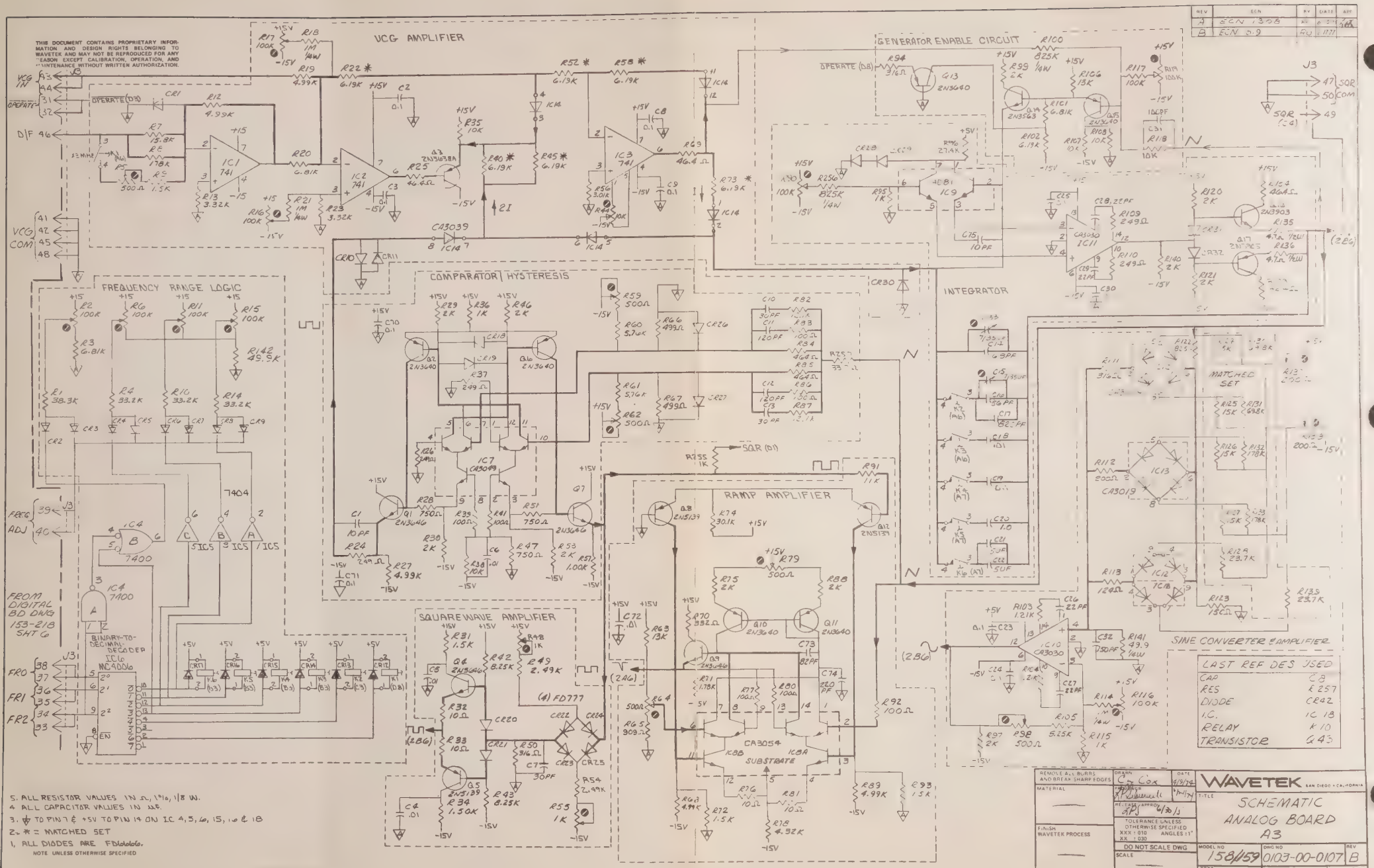
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROJ. ENGR	
	RELEASE APPROV.	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO, CALIFORNIA

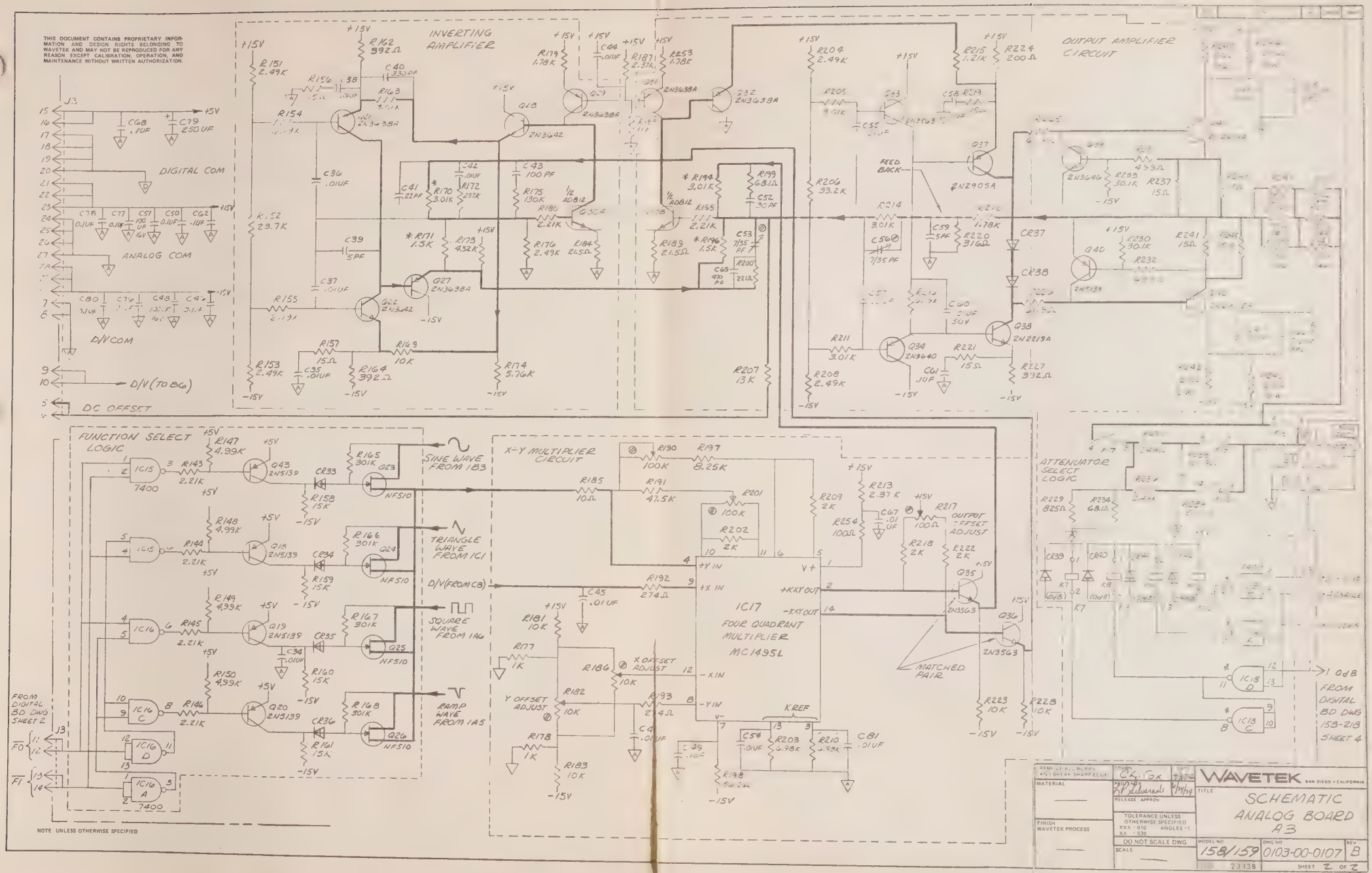
TITLE: DIGITAL

MODEL NO 58/159 | DWG NO 1100-00-0106 | REV B

CODE IDENT. 23330 | SHEET 1 OF 1


THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.
REV | ECN | BY | DATE | APP
A | ECN 1308 | KS | 6-2-76 | [illegible]
B | ECN 309 | RU | 11/77
UCG AMPLIFIER
GENERATOR ENABLE CIRCUIT
FREQUENCY RANGE LOGIC
COMPARATOR | HYSTERESIS
INTEGRATOR
RAMP AMPLIFIER
SQUAREWAVE AMPLIFIER
SINE CONVERTER & AMPLIFIER
MATCHED SET
SUBSTRATE
FROM DIGITAL BD DWG 153-218 SHT 6
BINARY-TO-DECIMAL DECODER IC16 MC4006
7404
7400
VCG IN
VCG COM
OPERATE
D/F
FREQ ADJ
FR0
FR1
FR2
SQR
SQR COM
LAST REF DES USED
CAP C8
RES R257
DIODE CR42
I.C. IC 18
RELAY K 10
TRANSISTOR Q45
5. ALL RESISTOR VALUES IN Ω, 1%, 1/8 W.
4 ALL CAPACITOR VALUES IN μF.
3. ⏚ TO PIN 7 & +5V TO PIN 14 ON IC 4, 5, 6, 15, 16 & 18
2. * = MATCHED SET
1. ALL DIODES ARE FD666666.
NOTE UNLESS OTHERWISE SPECIFIED
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN C. Cox 4/8/74
ENG APPROV 6/3/74
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 010 ANGLES ± 1° XX ± 030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO, CALIFORNIA
TITLE SCHEMATIC ANALOG BOARD A3
MODEL NO 158/159
DWG NO 0103-00-0107 REV B
CODE IDENT 23338
SHEET 1 OF 2

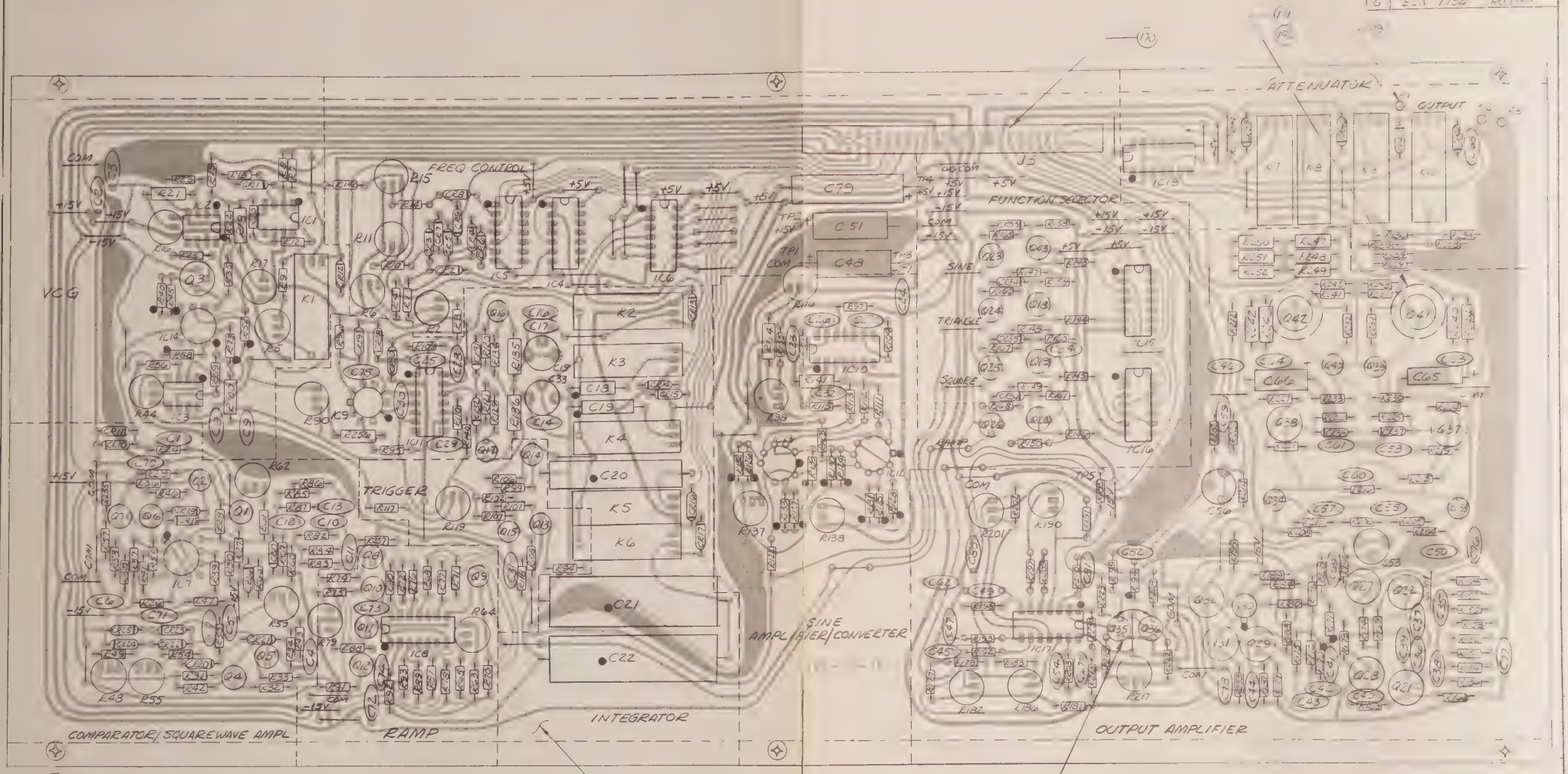
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



MATERIAL	DRAWN CK Fox 7/20/76	WAVETEK SAN DIEGO, CALIFORNIA	
FINISH WAVETEK PROCESS	RELEASE APPROV	TITLE SCHEMATIC ANALOG BOARD A3	
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XX ± .010 .XXX ± .030 ANGLES ± 1	MODEL NO 158/159	DWG NO 0103-00-0107 REV B
	DO NOT SCALE DWG	SCALE	SHEET 2 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV			BY	DATE	APP
E	ECN 1751				
F	ECN 1752				
G	ECN 1754				



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE SLIVERS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CA
MATERIAL —	ENG APPR		TITLE: P.C. BOARD ASSEMBLY ANALOG BD
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED .XX ± .010 .XXX ± .005 ANGLES ± 1°		MODEL NO 158/159
	DO NOT SCALE DWG	SCALE 2:1	DWG NO 010-00007 REV G
			CAGE IDENT 23338 SHEET 1 OF 1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DWG, ANALOG	0101-00-0107	WVTK	0101-00-0107	1
NONE	SCHEMATIC, ANALOG	0103-00-0107	WVTK	0103-00-0107	1
176	BAR,SUPPORT	158-312	WVTK	1400-00-0683	2
177	SHIELD	158-319	WVTK	1400-00-0703	1
C39 C59	CAP,CER,5PF,1KV	DD-050	CRL	1500-00-5011	2
C1 C75	CAP,CER,10PF,1KV	DD-100	CRL	1500-01-0011	2
C31 C43	CAP,CER,100PF,1KV	DD-101	CRL	1500-01-0111	2
C34 C35 C36 C37 C38 C4 C42 C44 C45 C47 C5 C54 C55 C57 C6 C60 C63 C64 C67 C81	CAP,CER,.01MF,50V	CK-103	CRL	1500-01-0310	20
C2 C23 C24 C25 C3 C30 C46 C49 C50 C58 C61 C62 C68 C70 C71 C72 C76 C77 C78 C8 C80 C9	CAP,CER,.1MF,20V	UK20-104	ARCO	1500-01-0413	22
C32	CAP,CER,150PF,1KV	DD-151	CRL	1500-01-5111	1
C26 C27 C28 C29 C41	CAP,CER,220PF,1KV	DD-220	CRL	1500-02-2011	5
C74	CAP,CER,220PF,1KV	DD-221	CRL	1500-02-2111	1
C52 C7	CAP,CER,30PF,1KV	DD-300	CRL	1500-03-0001	2
C40	CAP,CER,330PF,1KV	DD-331	CRL	1500-03-3111	1
C69	CAP,CER,470PF,1KV	DD-471	CRL	1500-04-7111	1

WAVETEK PARTS LIST | TITLE ANALOG | ASSEMBLY NO. 1100-00-0107 PAGE: 1 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	CAP,SET,POLYC CONSIST:1509-90-0001 THRU:0004			1509-80-0005	
C20	CAP,POLYC,.1MF,100V PART OF 1509-80-0005 QTY:0111500-41-0504				
C21 C22	CAP,POLYC,.5MF,100V PART OF 1509-80-0005 QTY:0211500-45-0504				
172	ANALOG	158-119	WVTK	1700-00-0107	1
170	CONN,HEADER 50 PIN	3433-4005	3M	2100-02-0029	1
190	PIN,MALE	61182-2	AMP	2100-05-0020	3
191	HEAT SINK	NF-207	WAKE	2800-11-0001	2
193	TRANSIPAD	10123N	METRS	2800-11-0003	2
192	TRANSIPAD	10160	METRS	2800-11-0004	2
K1 K10 K2 K3 K4 K5 K6 K7 K8 K9	RELAY,REED,FORM=A	RA3019-1051	ETHOL	4500-00-0007	10
W217	POT,TRIM,100	91AR100	BECK	4600-01-0103	1
W46 W55	POT,TRIM,1K	91AR1K	BECK	4600-01-0209	2
R182 R186 W44	POT,TRIM,10K	91AR10K	BECK	4600-01-0315	3
W11 R116 R119 R15 R16	POT,TRIM,100K	91AR100K	BECK	4600-01-0402	11

WAVETEK PARTS LIST | TITLE ANALOG | ASSEMBLY NO. 1100-00-0107 PAGE: 3 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R175	RES,MF,1/8W,1%,130K	RN55D-1303F	TRW	4701-03-1303	1
R123	RES,MF,1/8W,1%,150	RN55D-1500F	TRW	4701-03-1500	1
W31 R54 R72 W9 R93	RES,MF,1/8W,1%,1.5K	RN55D-1501F	TRW	4701-03-1501	5
R158 W159 W160 R161	RES,MF,1/8W,1%,15K	RN55D-1502F	TRW	4701-03-1502	4
W156 W157 R219 W221 R237 W241 R243 R245	RES,MF,1/8W,1%,15	RN55D-15R0F	TRW	4701-03-1509	8
R7	RES,MF,1/8W,1%,15.8K	RN55D-1582F	TRW	4701-03-1582	1
R179 W212 W253 R71	RES,MF,1/8W,1%,1.78K	RN55D-1781F	TRW	4701-03-1781	4
R8	RES,MF,1/8W,1%,178K	RN55D-1783F	TRW	4701-03-1783	1
W112 W224	RES,MF,1/8W,1%,200	RN55D-2000F	TRW	4701-03-2000	2
R120 W121 W140 W202 W204 R218 W222 R29 W30 W46 W53 R75 R88 R97 R99	RES,MF,1/8W,1%,2K	RN55D-2001F	TRW	4701-03-2001	15
R184 W189	RES,MF,1/8W,1%,21.5	RN55D-21R5F	TRW	4701-03-2159	2
R200	RES,MF,1/8W,1%,221	RN55D-2210F	TRW	4701-03-2210	1
W145 W144 W145 W146 W180 W195	RES,MF,1/8W,1%,2.21K	RN55D-2211F	TRW	4701-03-2211	8
W187 W213	RES,MF,1/8W,1%,2.37K	RN55D-2371F	TRW	4701-03-2371	2
W152	RES,MF,1/8W,1%,23.7K	RN55D-2372F	TRW	4701-03-2372	1

WAVETEK PARTS LIST | TITLE ANALOG | ASSEMBLY NO. 1100-00-0107 PAGE: 5 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C73	CAP,CER,82PF,1KV	DD-820	CRL	1500-08-2011	1
C11 C12	CAP,MICA,120PF,500V	DM15-121J	AMCO	1500-11-2100	2
C10 C13	CAP,MICA,30PF,500V	DM15-300J	AMCO	1500-13-0000	2
C16	CAP,MICA,56PF,500V	DM15-560J	AMCO	1500-15-6000	1
C14	CAP,MICA,68PF,500V	DM15-680F	AMCO	1500-16-8001	1
C17	CAP,MICA,820PF,300V	DM15-821F	ARCO	1500-18-2101	1
C48 C51	CAP,ELECT,100MF,16V	500D107G016DC7	SPRAG	1500-31-0101	2
C79	CAP,ELECT,250MF,16V	500D257G016DF7	SPRAG	1500-32-5101	1
C15 C33 C53 C56	VARI,7-35PF,250V	78-TWIKO-02 7/35 PF	TWIKO	1500-53-5000	4
C65 C66	CAP,TANT,5.6MF,35V	150D565X9035B2	SPRAG	1500-75-6502	2
	CAP,SET,POLYC CONSIST:1509-90-0001 THRU:0004	130-501-6	WVTK	1509-80-0005	1
C18	CAP,POLYC,.01MF,100V PART OF 1509-80-0005 QTY:0111500-41-0304				
C19	CAP,POLYC,.1MF,100V PART OF 1509-80-0005 QTY:0111500-41-0404				

WAVETEK PARTS LIST | TITLE ANALOG | ASSEMBLY NO. 1100-00-0107 PAGE: 2 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R17 R190 R2 R201 R6 W90					
R137 R138	POT,TRIM,200	91AR200	BECK	4600-02-0101	2
W5 R59 R62 R64 R79 R98	POT,TRIM,500	91AR500	BECK	4600-05-0104	6
R240 R242 R244 R246	RES,C,1/2W,5%,27	RC20GF-270	STKPL	4700-25-0270	4
R135 R136	RES,C,1/2W,5%,4.7	RC20GF-4R7	STKPL	4700-25-0479	2
W254 R39 R41 R77 R80 W83 R86 R92	RES,MF,1/8W,1%,100	RN55D-1000F	TRW	4701-03-1000	8
R115 R177 R178 R255 R36 R57 R95	RES,MF,1/8W,1%,1K	RN55D-1001F	TRW	4701-03-1001	7
R107 R108 R118 R169 R181 R183 W223 R228 R35 R38	RES,MF,1/8W,1%,10K	RN55D-1002F	TRW	4701-03-1002	10
R117	RES,MF,1/8W,1%,100K	RN55D-1003F	TRW	4701-03-1003	1
R185 R32 R33 W76 R81	RES,MF,1/8W,1%,10	RN55D-10R0F	TRW	4701-03-1009	5
R188 R91	RES,MF,1/8W,1%,11K	RN55D-1102F	TRW	4701-03-1102	2
W103 W104 R215	RES,MF,1/8W,1%,1.21K	RN55D-1211F	TRW	4701-03-1211	3
R82 R87	RES,MF,1/8W,1%,12.1K	RN55D-1212F	TRW	4701-03-1212	2
W113	RES,MF,1/8W,1%,124	RN55D-1240F	TRW	4701-03-1240	1
R106 W207 R63	RES,MF,1/8W,1%,13K	RN55D-1302F	TRW	4701-03-1302	3

WAVETEK PARTS LIST | TITLE ANALOG | ASSEMBLY NO. 1100-00-0107 PAGE: 4 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R172	RES,MF,1/8W,1%,237K	RN55D-2373F	TRW	4701-03-2373	1
R104 R110 W235 R26 R26 R37	RES,MF,1/8W,1%,249	RN55D-2490F	TRW	4701-03-2490	6
W151 W153 R176 W204 W208 W236 R49 W54	RES,MF,1/8W,1%,2.49K	RN55D-2491F	TRW	4701-03-2491	8
W192 R193	RES,MF,1/8W,1%,274	RN55D-2740F	TRW	4701-03-2740	2
R96	RES,MF,1/8W,1%,27.4K	RN55D-2742F	TRW	4701-03-2742	1
R163 W205 W211 R214 W56	RES,MF,1/8W,1%,3.01K	RN55D-3011F	TRW	4701-03-3011	5
R230 R233 R74	RES,MF,1/8W,1%,30.1K	RN55D-3012F	TRW	4701-03-3012	3
R165 R166 R167 R168	RES,MF,1/8W,1%,301K	RN55D-3013F	TRW	4701-03-3013	4
R111 W220 R50 R94	RES,MF,1/8W,1%,316	RN55D-3160F	TRW	4701-03-3160	4
R70	RES,MF,1/8W,1%,332	RN55D-3320F	TRW	4701-03-3320	1
R13 R23	RES,MF,1/8W,1%,3.32K	RN55D-3321F	TRW	4701-03-3321	2
R10 R14 R206 R6	RES,MF,1/8W,1%,33.2K	RN55D-3322F	TRW	4701-03-3322	4
R257	RES,MF,1/8W,1%,33.2	RN55D-33R2F	TRW	4701-03-3329	1
R1	RES,MF,1/8W,1%,38.3K	RN55D-3832F	TRW	4701-03-3832	1
R162 R164 R227	RES,MF,1/8W,1%,392	RN55D-3920F	TRW	4701-03-3920	3
W173 W78	RES,MF,1/8W,1%,4.32K	RN55D-4321F	TRW	4701-03-4321	2

WAVETEK PARTS LIST | TITLE ANALOG | ASSEMBLY NO. 1100-00-0107 PAGE: 6 | REV F

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ANALOG
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° .XX ± .030		
	DO NOT SCALE DWG		MODEL NO 158/159 · DWG NO 1100-00-0107 · REV F
	SCALE		CODE IDENT 23338 · SHEET OF 2

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R84 R85	RES,MF,1/8W,1%,464	RN55D-4640F	TRW	4701-03-4640	2
R124 R134 R25 R89	RES,MF,1.8W,1%,46.4	RN55D-46R4F	TRW	4701-03-4649	4
R191	RES,MF,1/8W,1%,47.5K	RN55D-4752F	TRW	4701-03-4752	1
R231 R232 R66 R67	RES,MF,1/8,1%,499	RN55D-4990F	TRW	4701-03-4990	4
R12 R147 R148 R149 R150 R19 R27 R68 R89	RES,MF,1/8W,1%,4.99K	RN55D-4991F	TRW	4701-03-4991	9
R142	RES,MF,1/8W,1%,49.9K	RN55D-4992F	TRW	4701-03-4992	1
R239	RES,MF,1/8W,1%,51.1	RN55D-51R1F	TRW	4701-03-5119	1
R198	RES,MF,1/8W,1%,56.2	RN55D-56R2F	TRW	4701-03-5629	1
R170 R60 R61	RES,MF,1/8W,1%,5.76K	RN55D-5761F	TRW	4701-03-5761	3
R102 R150 R155 R216	RES,MF,1/8W,1%,6.19K	RN55D-6191F	TRW	4701-03-6191	4
R225 R226 R238	RES,MF,1/8W,1%,61.9	RN55D-61R9F	TRW	4701-03-6199	3
R101 R20 R3	RES,MF,1/8W,1%,6.81K	RN55D-6811F	TRW	4701-03-6811	3
R199 R234	RES,MF,1/8W,1%,68.1	RN55D-68R1F	TRW	4701-03-6819	2
R203 R210	RES,MF,1/8W,1%,6.98K	RN55D-6981F	TRW	4701-03-6981	2
R28 R47 R51	RES,MF,1/8W,1%,75U	RN55D-7500F	TRW	4701-03-7500	3
R229	RES,MF,1/8W,1%,825	RN55D-8250F	TRW	4701-03-8250	1
R105 R197 R42 R43	RES,MF,1/8W,1%,8.25K	RN55D-8251F	TRW	4701-03-8251	4

WAVETEK PARTS LIST	TITLE ANALOG	ASSEMBLY NO. 1100-00-0107 PAGE: 7	REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	RES,MF,SET,MATCHED CONSIST:4799-00-0026 THRU:0029			4789-00-0032	
R130 R131	RES,MF,1/8W,1%,69.8K PART OF 4789-00-0032 QTY:02:4701-03-6982				
R132 R133	RES,MF,1/8W,1%,178K PART OF 4789-00-0032 QTY:02:4701-03-1783				
CR22 CR23 CR24 CR25	DIODE	FD-777	FAIR	4807-02-0777	4
CR1 CR10 CR11 CR12 CR13 CR14 CR15 CR16 CR17 CR18 CR19 CR2 CR20 CR21 CR26 CR27 CR28 CR29 CR3 CR30 CR31 CR32 CR33 CR34 CR35 CR36 CR37 CR38 CR39 CR4 CR40 CR41 CR42 CR5 CR6 CR7 CR8 CR9	DIODE	FD-6666	FAIR	4807-02-6666	38
Q38 Q41	TRANS	2N2219A	FAIR	4901-02-2191	2
Q37 Q42	TRANS	2N2905A	FAIR	4901-02-9051	2
Q14 Q35	TRANS	2N3563	FAIR	4901-03-5630	2
Q21 Q27 Q29 Q3 Q31 Q32	TRANS	2N3638A	FAIR	4901-03-6381	6
Q10 Q11 Q13 Q15 Q2	TRANS	2N3640	FAIR	4901-03-6400	7

WAVETEK PARTS LIST	TITLE ANALOG	ASSEMBLY NO. 1100-00-0107 PAGE: 9	REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
IC10	IC,CLASS II,CA-3030 QTY:1:17000-30-3000	130-501-16	WVTK	7200-00-0002	1
IC14	IC,CLASS I,CA-3039 QTY:1:17000-30-3900	130-501-18	WVTK	7200-00-0004	1
IC6	IC	4006	MOT	8000-40-0600	1
IC15 IC16 IC4	IC	7400	TI	8000-74-0000	3
IC18	IC	7403	TI	8000-74-0300	1
IC5	IC	7404	TI	8000-74-0400	1

WAVETEK PARTS LIST	TITLE ANALOG	ASSEMBLY NO. 1100-00-0107 PAGE: 11	REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R122	RES,MF,1/8W,1%,82.5	RN55D-82R5F	TRW	4701-03-8259	1
R65	RES,MF,1/8W,1%,909	RN55D-9090F	TRW	4701-03-9090	1
R114 R18 R21	RES,MF,1/4W,1%,1M	RN60D-1004F	TRW	4701-13-1004	3
R141	RES,MF,1/4W,1%,49.9	RN60D-49R9F	TRW	4701-13-4999	1
R247 R248 R249 R250 R251 R252	RES,MF,1/4W,1%,75	RN60D-75R0F	TRW	4701-13-7509	6
R100 R256	RES,MF,1/4W,1%,825K	RN60D-8253F	TRW	4701-13-8253	2
M171 M196	RES,SET,2=1.5K,1/8W WTY:2:4701-03-1501	158-501-95A	WVTK	4789-00-0008	1
M170 M198	RES,SET,2=3.01K,1/8W WTY:2:4701-03-3011	157-501-28A	WVTK	4789-00-0012	1
R22 R40 R45 R52 R58 M73	RES,SET,6=6.19K,1/8W WTY:6:4701-03-6191	130-501-3A	WVTK	4789-00-0016	1
	RES,MF,SET,MATCHED CONSIST:4799-00-0026 THRU:0029	130-501-5A	WVTK	4789-00-0032	1
R124 R125 R126 R127	RES,MF,1/8W,1%,15K PART OF 4789-00-0032 QTY:04:4701-03-1502				
R128 R139	RES,MF,1/8W,1%,23.7K PART OF 4789-00-0032 QTY:02:4701-03-2372				

WAVETEK PARTS LIST	TITLE ANALOG	ASSEMBLY NO. 1100-00-0107 PAGE: 8	REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q34 Q6					
Q22 Q28	TRANS	2N3642	FAIR	4901-03-6420	2
Q1 Q39 Q4 Q7 Q9	TRANS	2N3646	FAIR	4901-03-6460	5
Q16	TRANS	2N3903	FAIR	4901-03-9030	1
Q17	TRANS	2N3905	FAIR	4901-03-9050	1
Q12 Q18 Q19 Q20 Q40 Q43 Q5 Q8	TRANS	2N5139	FAIR	4901-05-1390	6
Q23 Q24 Q25 Q26	TRANS	NF-510	NSC	4902-00-5100	4
Q35 Q36	TRANS,M/PR,2N3563 WTY:2:4901-03-5630	142-501-52	WVTK	4998-00-0004	1
IC1 IC2 IC3	IC	MA-741	FAIR	7000-07-4100	3
IC9	IC	AD 811	ANDEV	7000-08-1100	1
Q30	IC	AD 812	ANDEV	7000-08-1200	1
IC17	IC	MC1495L	MOT	7000-14-9500	1
IC12 IC13	IC	CA-3019	RCA	7000-30-1900	2
IC7	IC	CA-3049	RCA	7000-30-4900	1
IC8	IC	CA-3054	RCA	7000-30-5400	1
IC11	IC,CLASS I,CA-3030 QTY:1:17000-30-3000	130-501-15	WVTK	7200-00-0001	1

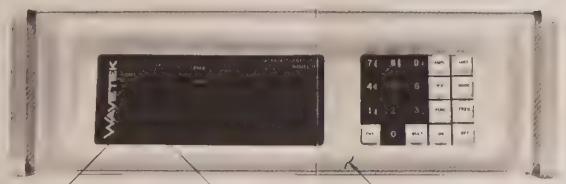
WAVETEK PARTS LIST	TITLE ANALOG	ASSEMBLY NO. 1100-00-0107 PAGE: 10	REV F

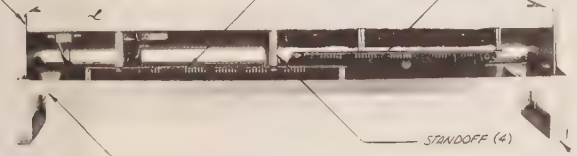
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ANALOG
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG		MODEL NO 158/159 DWG NO 1100-00-0107 REV F
	SCALE		CODE IDENT 23338 SHEET 2 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

LTR	DESCRIPTION	BY	DATE	APP'D
A	CHG DWG NO. FROM 159-001 ECN 115	[illegible]	9/67	
B	ECN 1160	RD	11/68	
C	ADD ASSY WAS 158-016 DELETED ITEM 10 154-331 ECN 1131	[illegible]	1/7	
D	ECN 1288	RD	6/25/73	
E	ECN 1754	RD	12/78	





(6) BRACKET (2)
POP RIVET SUB PANEL TO BRACKET (4 PLCS)
(2) SUB PANEL
DISPLAY BOARD
KEYBOARD
STANDOFF (4)
(8) TRIM (2)
(REF) ▽
(7) HANDLE (2)
(16) HANDLE TRIM (2)
PUSH BUTTON
(3) PANEL PLEX
(1) FRONT PANEL
(14) SHIM SPACER (2) ▽
1/4" DOUBLE SIDED ADHESIVE TAPE.

▽ INSTALL SHIM SPACER BEHIND FRONT PANEL USING V4" DOUBLE SIDED TAPE, BEFORE ADDING TRIM.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CL Cox	DATE 5/6/70
MATERIAL ——	PROJ ENGR RP Schwenke	4-4-70
	RELEASE APPROV JPS	6/30/70
FINISH WAVETEK PROCESS ——	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ± 1	
	DO NOT SCALE DWG	
	SCALE NONE	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
ASSEMBLY
FRONT PANEL

MODEL NO	DWG NO	REV
159	0102-00-0333	E

CODE IDENT 23338 SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	DWG-MFGR-PART-NO	MFGR	WAVETEK NO.	
NONE	ASSY DWG, FRONT PNL	0102-00-0333	WVTK	0102-00-0333	
1	PANEL,FT REF:3200-03-0002	158-309	WVTK	1400-00-0660	
3	PANEL,PLEX	158-318	WVTK	1400-00-0690	
4	PANEL,SUB	158-323	WVTK	1400-00-0723	
5	BRKT	158-324	WVTK	1400-00-0733	
7	HANDLE,W/A FROM:1400-00-3561	147-368	WVTK	1400-00-3589	
16	TRIM,HANDLE REF:3200-06-0006	147-345	WVTK	1400-00-3619	
17	SHIM,SPACER	1400-00-7003	WVTK	1400-00-7003	
18	TRIM REF:3200-06-0005	1400-00-7019	WVTK	1400-00-7019	
[illegible]	SPACER	8221-A-0632	AMTOM	2800-02-0012	

WAVETEK PARTS LIST

TITLE
FT PANEL ASSY

ASSEMBLY NO
1101-00-0075

REV.
E

Weight: [illegible]

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: FRONT PANEL ASSY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1° XX ± .030		
	DO NOT SCALE DWG		MODEL NO 159 / DWG NO 1101-00-0075 / REV E
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

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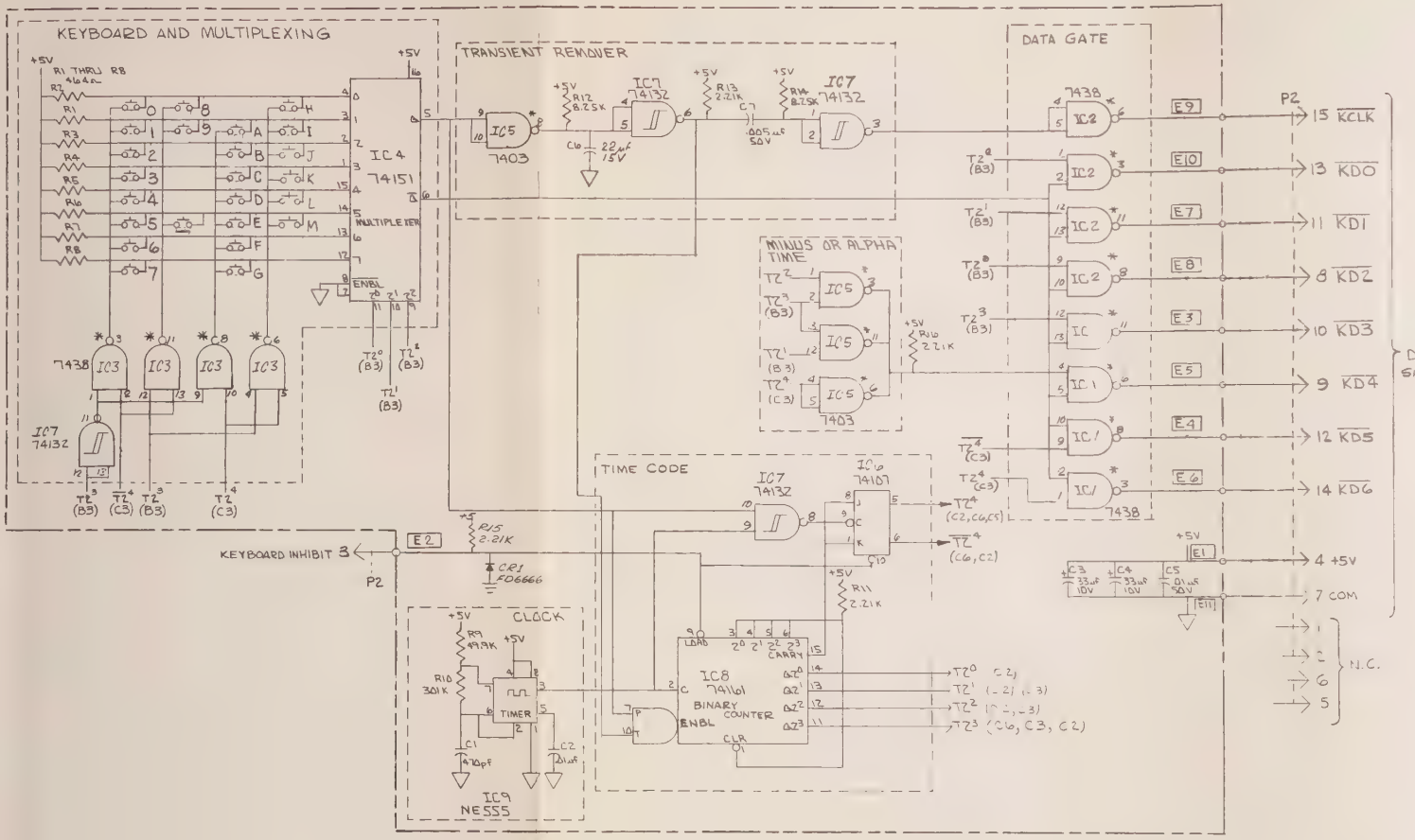
REV	ECN	BY	DATE	APP
A	ECN 1754	RD	6-20-2	

KEYBOARD ARRANGEMENT

7	8	9	F	G
4	5	6	A	C
1	2	3	D	B
~	0	E	H	I

A = AMPL
B = MODE
C = FUNC
D = OFST
E = MULT
F = FREQ
G = UNIT
H = ON
I = OFF
~ = CHS



5. ○ DENOTES WIRE COLORS PER RESISTOR COLOR CODES.
4. ▭ DENOTES ACTUAL LABELING.
3. BAR OVER MNEMONIC DENOTES TRUE-WHEN-LOW.
2. * DENOTES OPEN COLLECTOR.
1. ALL RESISTORS ARE ±1% ⅛W.

NOTE: UNLESS OTHERWISE SPECIFIED.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Gary T	DATE 1/19
MATERIAL	PROGRAMMER B.P. Silvernail	DATE 1/8/75
FINISH WAVETEK PROCESS	RELEASED JRS	DATE NOV
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC KEY BOARD A6

MODEL NO	DWG NO	REV
159	0103-00-0109	A

CODE IDENT 23338 SHEET 1 OF 1

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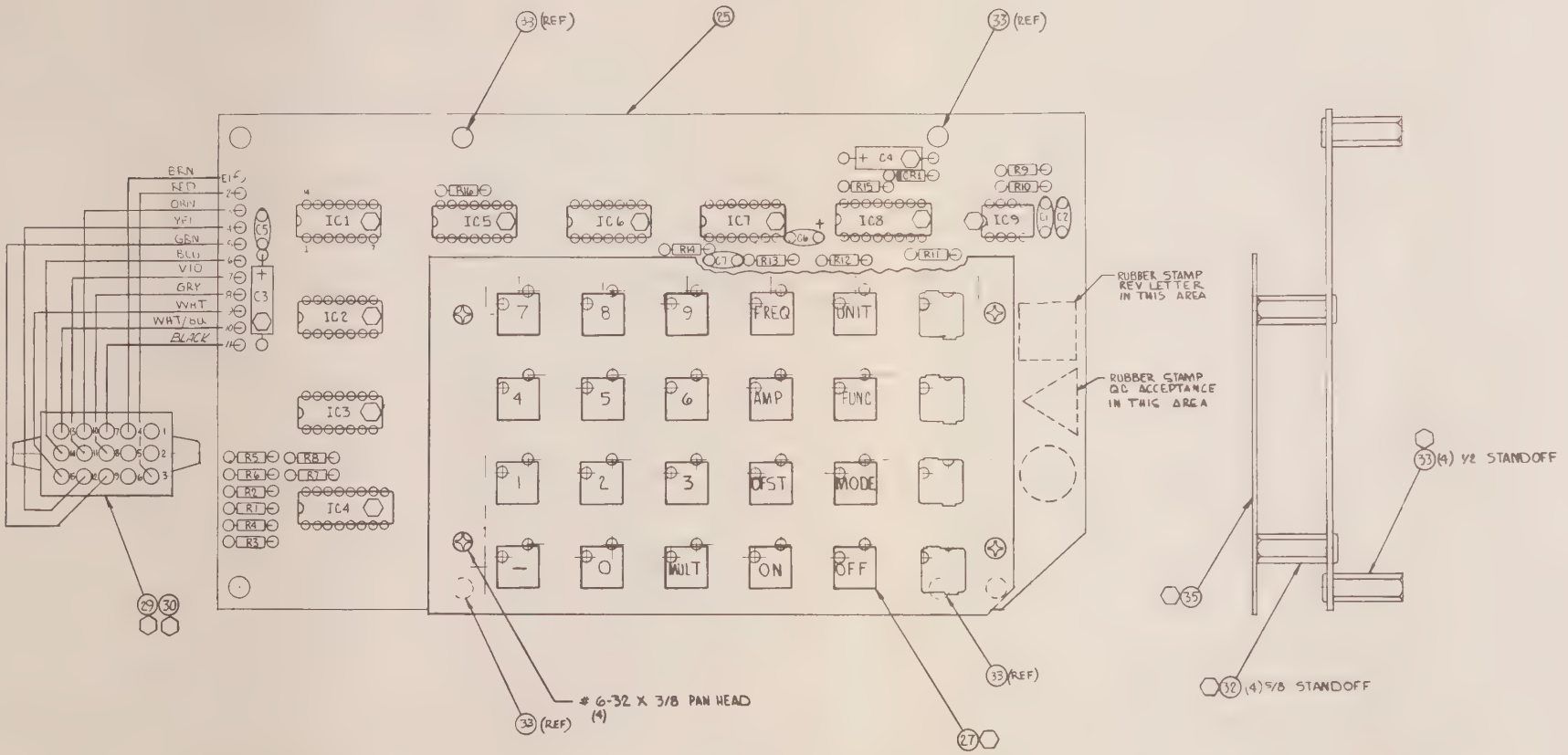
REV	E'N	BY	DATE	APP
A	ECN 1754	PO	6-8-78	



1. ⑥ NUMBERS IN HEX AND CIRCLES INDICATE STATION LOCATION.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. BARNETT	DATE 12/11/78	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	ENGINEER [signature]	1/7/79	TITLE PC ASSY- KEYBOARD
FINISH WAVETEK PROCESS	RELEASE APP		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ± 1		
	DO NOT SCALE DWG	MODEL NO 159	DWG NO 0101-00-0109 REV A
	SCALE 2/1	CODE IDENT 23338	SHEET 1 OF 1

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, KEYBOARD	0101-00-0109	WVTK	0101-00-0109	1
NONE	SCHEMATIC, KEYBOARD	0103-00-0109	WVTK	0103-00-0109	1
35	CARRIER,KEY	158-344	WVTK	1400-00-0783	1
C2 C5	CAP,CER,.01MF,50V	CK-103	CRL	1500-01-0310	2
C1	CAP,CER,470PF,1KV	DD-471	CRL	1500-04-7111	1
C7	CAP,CER,.005MF,50V	CK-502	CRL	1500-05-0210	1
C6	CAP,TANT,22MF,15V	196D226X9015KA1	SPRAG	1500-72-2601	1
C3 C4	CAP,TANT,.33MF,10V	150D336X9010B2	SPRAG	1500-73-3601	2
25	KEY BOARD	158-147	WVTK	1700-00-0109	1
30	PLUG,15PIN	03-09-2151	MOLEX	2100-02-0013	1
29	PIN,MALE	02-09-2118	MOLEX	2100-05-0005	11
33	STANDOFF	15318-1/2-11	USECO	2800-02-0003	4
32	STANDOFF	15318-5/8	USECO	2800-02-0004	4
R11 R13 R15 R16	RES,MF,1/8W,1%,2.21K	RN55D-2211F	TRW	4701-03-2211	4
R10	RES,MF,1/8W,1%,301K	RN55D-3013F	TRW	4701-03-3013	1
R1 R2 R3 R4 R5 R6 R7 R8	RES,MF,1/8W,1%,464	RN55D-4640F	TRW	4701-03-4640	8
R9	RES,MF,1/8W,1%,49.9K	RN55D-4992F	TRW	4701-03-4992	1

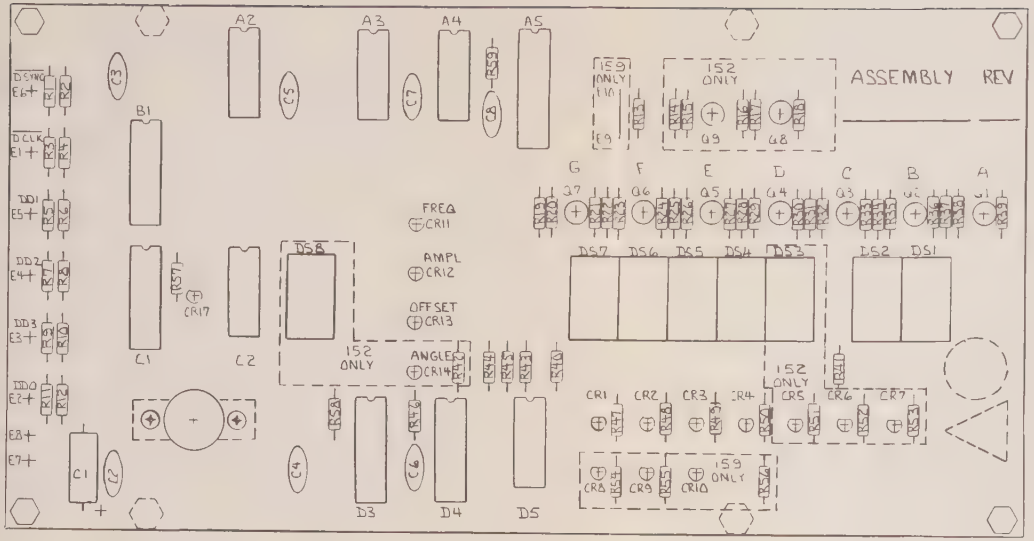
WAVETEK PARTS LIST	TITLE KEY BOARD	ASSEMBLY NO. 1100-00-0109 PAGE: 1	REV A

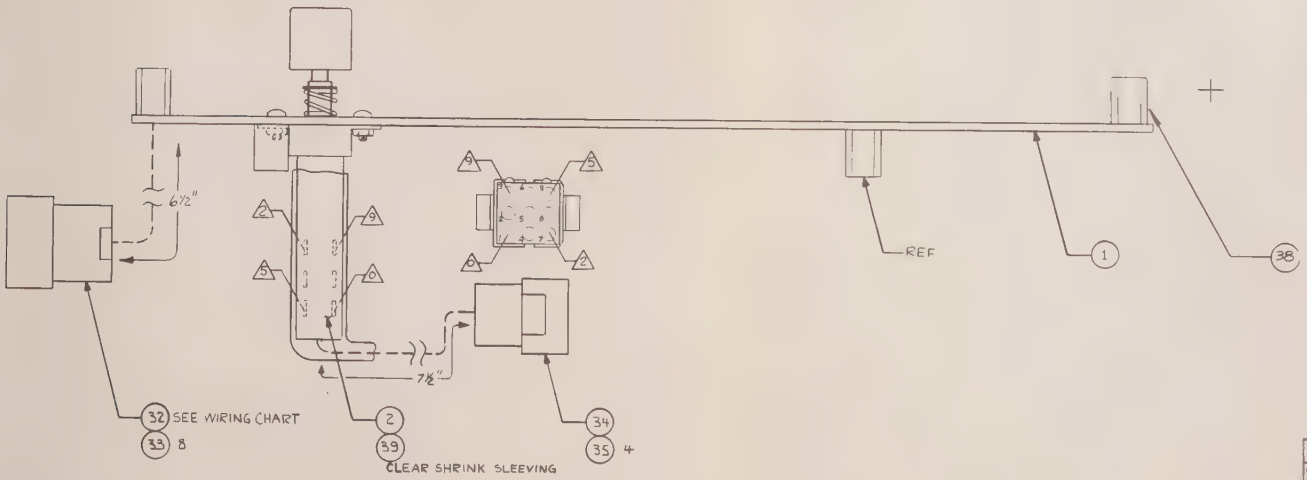
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R12 R14	RES,MF,1/8W,1%,8.25K	RN55D-8251F	TRW	4701-03-8251	2
CR1	DIODE	FD-6666	FAIR	4807-02-6666	1
27	KEY & SWITCH KIT	159-531	WVTK	5108-00-0001	1
IC9	IC	NE555V	SIG	7000-05-5500	1
IC5	IC	7403	TI	8000-74-0300	1
IC1 IC2 IC3	IC	7438	TI	8000-74-3800	3
IC6	IC	74107	TI	8007-41-0700	1
IC7	IC	74132	TI	8007-41-3200	1
IC4	IC	74151	TI	8007-41-5100	1
IC8	IC	74161	TI	8007-41-6100	1

WAVETEK PARTS LIST	TITLE KEY BOARD	ASSEMBLY NO. 1100-00-0109 PAGE: 2	REV A

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE KEYBOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 .XX ±.030 ANGLES ±1°		
	DO NOT SCALE DWG	MODEL NO. 159	DWG NO. 1100-00-0109 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

WIRING CHART		
BOARD LOCATION	CODED WIRE COLOR	CONNECTOR PIN NUMBER
E1	1	8
E2	2	10
E3	3	14
E4	4	11
E5	5	15
E6	6	13
E7	0	7
E8	7	4


158-152 DISPLAY BOARD SILKSCREEN MASTER
ASSEMBLY REV
152 ONLY
159 ONLY
FREQ CR11
AMPL CR12
OFFSET CR13
ANGLE CR14
DS1 DS2 DS3 DS4 DS5 DS6 DS7
A1 A2 A3 A4 A5
B1
C1 C2 C3 C4 C5 C6 C7 C8
D3 D4 D5
CR1 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9 CR10
G A B C D E F G



NOTES: 1. △DENOTES WIRE COLOR PER COLOR CODE.

		A	ECN 1314	RO 6-23-77 RP
	DRAWN HAAG	DATE 5-9-75	WAVETEK	
MATERIAL SEE PARTS LIST	ENGINEER [signature]	DATE 5/14/75	TITLE SILKSCREEN ASSEMBLY DWG - DISPLAY BOARD	
	RELEASE APPROVED [signature]	DATE 6/24/75		
	SCALE 2/1		MODEL NO.	DWG NO. 0101-00-0105 REV A
			CODE IDENT 23338	SHEET 1 OF 3

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DWNG, DISPLAY	0101-00-0105	WVTK	0101-00-0105	1
NONE	SCHEMATIC, DISPLAY	0103-00-0105	WVTK	0103-00-0105	1
C2 C3 C4 C5 C6 C7 C8	CAP,CER,.01MF,50V	CK-103 LONG LEAD	CRL	1500-01-0300	7
C1	CAP,TANT,33MF,10V	150D336X9010B2	SPRAG	1500-73-5601	1
1	DISPLAY	158-151	WVTK	1700-00-0105	1
J4	PLUG,9PIN	03-06-2091	MOLEX	2100-02-0011	1
J2	PLUG,15PIN	03-09-2151	MOLEX	2100-02-0013	1
J5	PIN,MALE	02-06-2103	MOLEX	2100-05-0003	4
J3	PIN,MALE	02-04-2118	MOLEX	2100-05-0005	8
J8	STANDOFF	6910-6-2C	LYNTK	2800-03-0002	4
R13 R21 R24 R27 R30 R33 R36 R39	RES,MF,1/8W,1%,15	RN55D-15R0F	TRW	4701-03-1509	8
R1 R11 R3 R5 R7 R9	RES,MF,1/8W,1%,221	RN55D-2210F	TRW	4701-03-2210	6
R46 R58 R59	RES,MF,1/8W,1%,2.21K	RN55D-2211F	TRW	4701-03-2211	3
R40 R41 R43 R44 R45 R47 R48 R49 R50 R54 R55 R56 R57	RES,MF,1/8W,1%,274	RN55D-2740F	TRW	4701-03-2740	13
R10 R12 R19 R2 R22 R25 R28 R31 R34 R37 R4 R6 R8	RES,MF,1/8W,1%,332	RN55D-3320F	TRW	4701-03-3320	13

WAVETEK PARTS LIST	TITLE DISPLAY	ASSEMBLY NO. 1100-00-0105 PAGE: 1	REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R20 R23 R26 R29 R32 R35 R38	RES,MF,1/8W,1%,6.81K	RN55D-6811F	TRW	4701-03-6811	7
CR1 CR10 CR11 CR12 CR13 CR17 CR2 CR3 CR4 CR8 CR9	LED	TIL-209A	TI	4899-00-0005	11
DS1 DS2 DS4 DS5 DS6 DS7	LED	5082-7740-L	HP	4899-00-0009	6
Q1 Q2 Q3 Q4 Q5 Q6 Q7	TRANS	2N5640	FAIR	4901-03-6400	7
S2	SWITCH ASSY P8	157-422	WVTK	5103-00-0011	1
S9	BUTTON	6315 BLACK	CRL	5103-04-0001	1
ICD5	IC	4006	MOT	8000-40-0600	1
ICA3	IC	7400	TI	8000-74-0000	1
ICC2	IC	7438	TI	8000-74-3800	1
ICA2	IC	7474	TI	8000-74-7400	1
ICA5	IC	DS8863	NSC	8000-88-6300	1
ICB1	IC	9370DC	FAIR	8000-93-7000	1
ICA4	IC	74164	TI	8007-41-6400	1
ICC1 ICD3 ICD4	IC	74175	TI	8007-41-7500	3

WAVETEK PARTS LIST	TITLE DISPLAY	ASSEMBLY NO. 1100-00-0105 PAGE: 2	REV B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE DISPLAY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°		
	DO NOT SCALE DWG		MODEL NO 158/159
	SCALE		DWG NO 1100-00-0105 REV B
			CODE IDENT 23338 SHEET 1 OF 1

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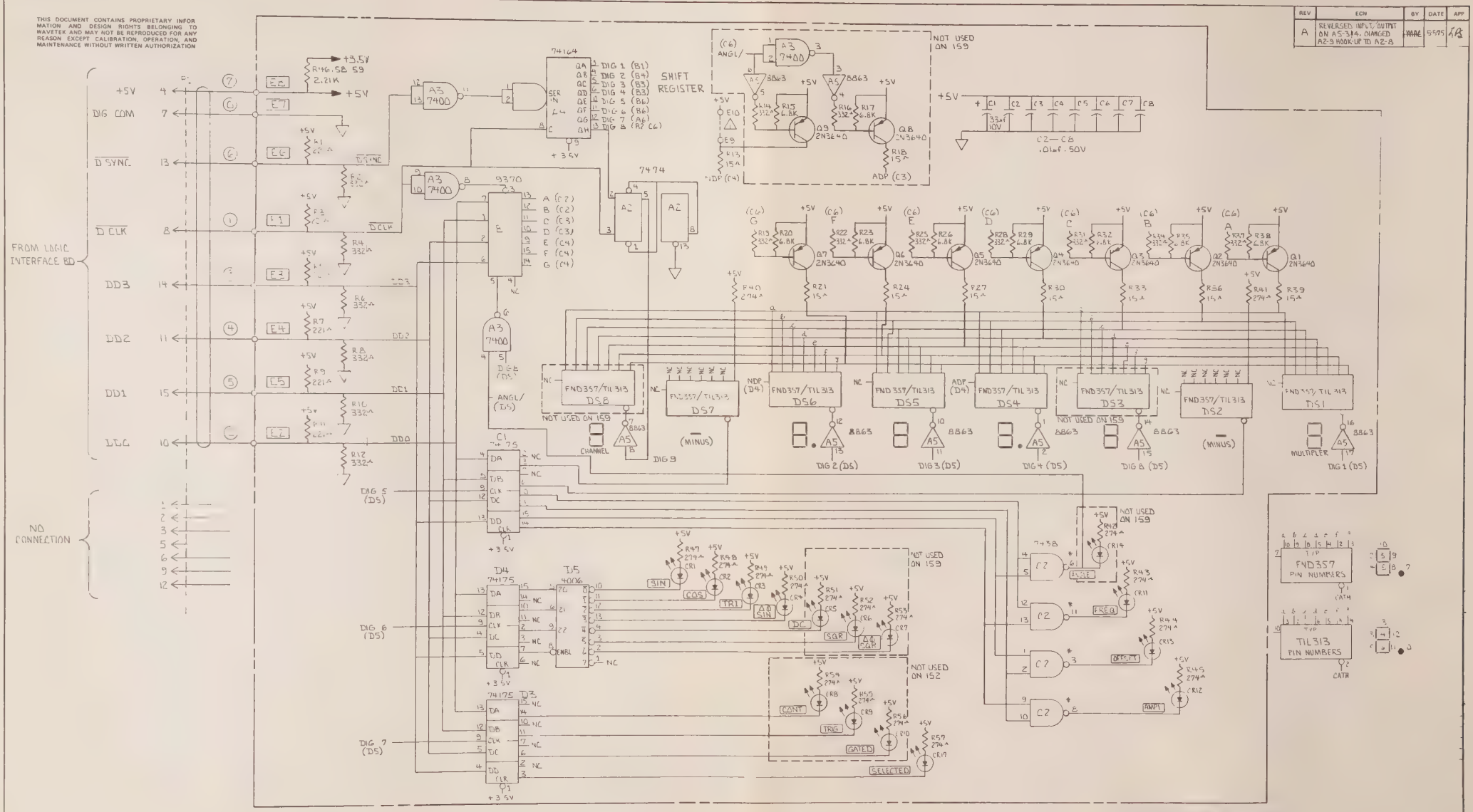
REV	ECN	BY	DATE	APP
A	REVERSED INPUT/OUTPUT ON AS-314, CHANGED A2-9 HOOK-UP TO A2-8	MAE	5-5-75	



4. ○ DENOTES WIRE COLOR PER COLOR CODE
3. ▭ DENOTES LABELING ON BOARD OR DISPLAY PANEL.
2. ALL RESISTORS ARE ±1% · ⅛W
1. △ ADD JUMPER WHEN LOADING FOR MODEL 159

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN MAE DATE 4-3-75
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.020
DO NOT SCALE DWG
SCALE —

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC— DISPLAY BOARD

MODEL NO 152/159 | DWG NO 0103-00-0105 | REV A | FSCM IDENT 23338 | SHEET 1 OF 1

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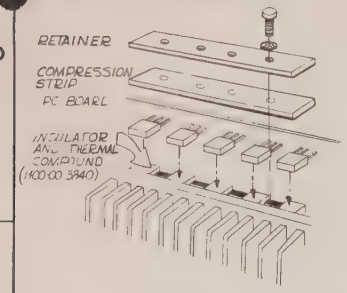
REV	ECN	BY	DATE	APP
A	ECN 1318	RD		
B	ECN 425	RD		
C	ECN 754			



DETAIL "A"

SEE POWER SUPPLY (1100-00-0108) FOR INSTALLATION OF Q1, Q6, Q7 & Q8 (LEADS MUST BE FULL LENGTH)

Q6 Q1 Q8

SW1 SW2

FASTEN BOTH SWITCHES WITH 4EA 4-40 X 1/4 PAN HEAD & #4 MIN LOCKWASHER & #4 MIN NUT

2EA 4-40 X 1/2 BLACK OXIDE PAN HEAD & #4 MIN. LOCKWASHER & #4 MIN NUT.

SAFETY EARTH GROUND LUG

50A OUT | SYNC OUT | TRIG IN | VCG IN

ADD NYLON SHOULDER WASHERS. (TYP 4 PLACES)

(REF) (11) (1)
(REF) (12) (4)
(REF) (13) (4)
(14) (4) (REF)

(17) AMP FAR END (3)

(17) AMP FAR END (6)

AT FINAL ASSY THIS CONN IS FROM DIGITAL BD. (158-078)

(15) (3)

1204-00-0481

WAVETEK

(10) REF

SECURE TRANSFORMER WITH 4 EA 8-32 X 2 1/4 PAN HEAD BLK OXIDE & #8 NUT & LOCKWASHER. (2 EA GO THRU BOARD)

SEE DETAIL "A"

COMPRESSION STRIP

2 EA 6-32 X 1/2 PAN HEAD BLACK OXIDE & 2 EA #6 NUT AND LOCK WASHER

SECURE TRANSISTORS WITH 4EA #6-32 X 3/4 PAN HEAD AND #6 LOCK WASHER

(30) (REF) WAKEFIELD COMPOUND (TYP 4 PL)

(23) (4) (REF)

(22) (REF)

1. NUMBERS INDICATE WIRE COLORS

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN ADKINS	DATE 8-2-74	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY POWER SUPPLY (REAR CASTING)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1° XX ± .030		
	DO NOT SCALE DWG		MODEL NO 158
	SCALE		DWG NO 0102-00-0332 REV E
			CODE IDENT 23338 SHEET 1 OF 2

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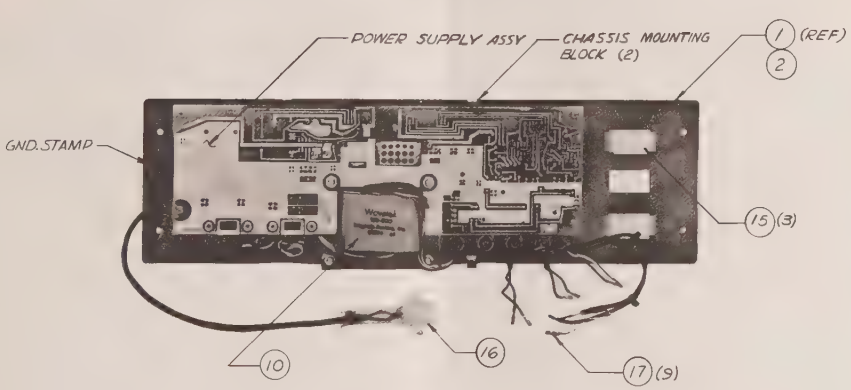
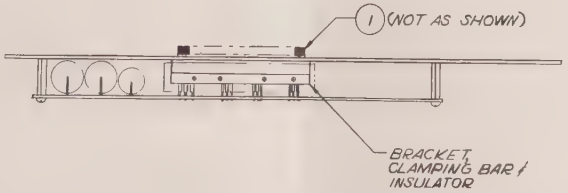
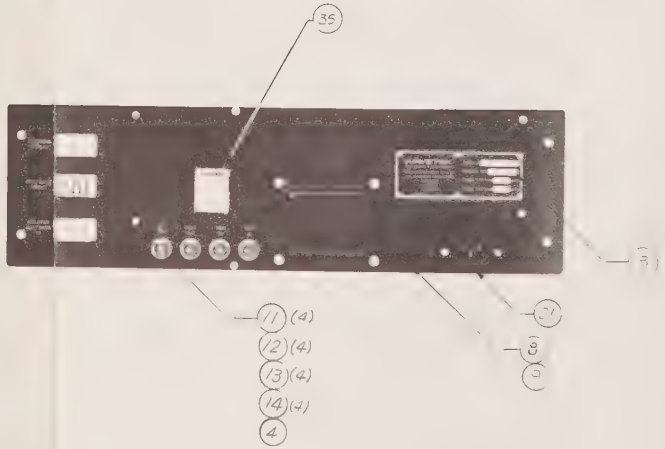
REV	ECN	BY	APP	DATE
A	DDC #1463	DC		4-6-83

SEE SHEET 1







NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN C.L. Cox	DATE 3/4/83	WAVETEK SAN DIEGO, CALIF.
MATERIAL —	APPROV	RELEASE APPROV	TITLE ASSEMBLY REAR PANEL
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES ±1 XX .030		
	DO NOT SCALE DWG	SCALE NONE	MODEL NO 158/159 DWG NO 0102-00-0332 REV E
			DCN 23338 SHEET 2 OF 2

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REFERENCE DESIGNATIONS	PART DESCRIPTION	MFG-PN-PART-NO	MFGR	MANUFACTURER'S NO.	QTY
A**	ASSY DWG, REAR PNL	0102-00-0352	WVTK	0102-00-0352	1
A*	TMA,STUMMER	152-5006	WVTK	1204-00-0001	1
C	EXTENDER	150-322	WVTK	1400-00-0710	1
C	LABEL,MEAN FROM:1400-00-3271	150-335	WVTK	1400-00-0734	1
CR	INSULATOR	147-367	WVTK	1400-00-3705	1
CR	PAN,CLAMP	147-374	WVTK	1400-00-3733	1
CR	DELAY,DNL	162-369	WVTK	1400-00-3813	1
CR	STRIP,CLAMP REF:1400-00-3733	162-312	WVTK	1400-00-3944	1
FUSE	LABEL,OPTION	1400-00-0800	WVTK	1400-00-0800	1
G	I.D. LABEL	1400-00-9110	WVTK	1400-00-9110	1
J1	BNC CONN	RL-7446	KING	2100-01-0002	1
J10	CONN,9PIN	03-09-1641	MOLEX	2100-02-0010	1
J15	CONN,15PIN	03-09-1151	MOLEX	2100-02-0012	1
J21	RECEPT,PWREM	EAC-301	SACFT	2100-03-0005	1
J4	SOLDER LUG	1497	SMITH	2100-04-0012	4
J**	SOLDER LUG	1485-E	SMITH	2100-04-0029	2
J9	PIN,FEMALE	02-09-1103	MOLEX	2100-05-0002	1

WAVETEK PARTS LIST	TITLE REAR PANEL ASSY	ASSEMBLY NO 1101-00-0074	REV F
		PAGE 1	

REFERENCE DESIGNATIONS	PART DESCRIPTION	MFG-PN-PART-NO	MFGR	MANUFACTURER'S NO.	QTY
J7	CONN	80598-2	AMP	2100-05-0017	1
J8	PIN,FEMALE	02-09-1118	MOLEX	2100-05-0020	1
F	FUSE,2500V,3/4A,SB	313-750	LITEL	2400-05-0011	1
F	FUSE HOLD	031.1853/031.1000	SCHUR	2400-05-0012	1
C1	SPEED/VOL,TYPE"U"	C16C50-B3C-A	TINN	2800-00-0	1
J2	WASHER,SHOULDER	2060	SMITH	2800-27-0004	4
J4	NYLON FLAT WASHER	2004-N-389	AMIUM	2800-28-0005	4
J9	DA ASST SLIDE PI-LU	SHW22-FI-MK	UID	5105-00-0001	1
C1	SMITH ASST SLIDE	WC25E-LP	SACFT	5105-00-0006	1
S1	SOLDER GUARD	WC25E-LP-SG	SACFT	5105-00-0	1

WAVETEK PARTS LIST	TITLE REAR PANEL ASSY	ASSEMBLY NO 1101-00-0074	REV F
		PAGE 2	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHK'D/APVD		TITLE PARTS LIST REAR PANEL ASSY
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX .030		
	DO NOT SCALE DWG		MODEL NO 159 DWG NO 1101-00-0074 REV F
	SCALE		CODE IDENT 23338 SHEET 1 OF

© SHOP GRAPHICS/ACCUPRESS REORDER NO. A 3894

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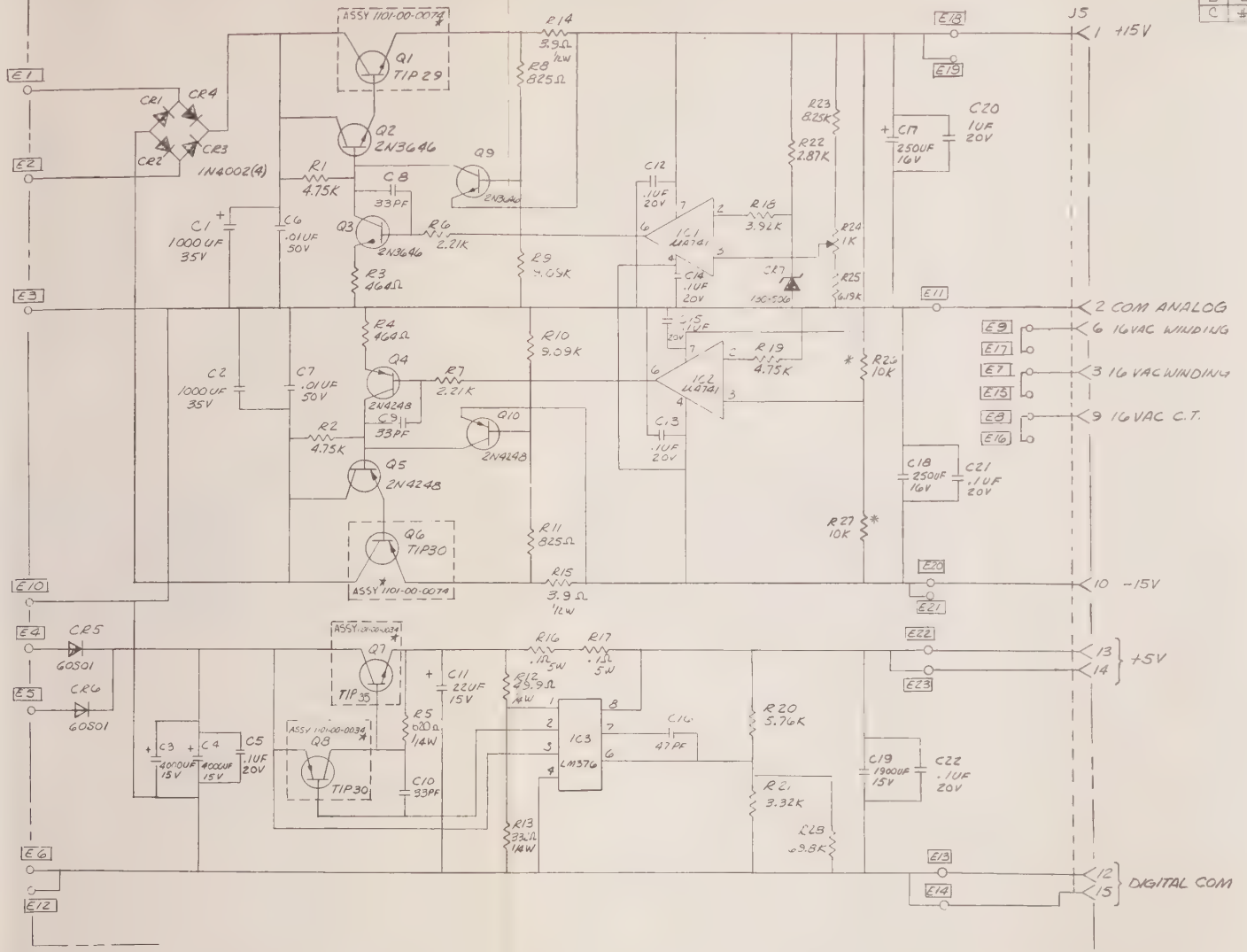
REV.	ECN			
A	1069			
B	ECN 1754			
C	# 1920			



3. ☆ ATTACHED TO REAR PANEL HEATSINK BRACKET.
2. * INDICATES MATCHED SET.
1. ALL RESISTORS ARE 1/8W 1%.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CL Fox 9/25/84	WAVETEK SAN DIEGO, CAL
MATERIAL	PROJ ENG [signature] 9/27/84	TITLE SCHEMATIC POWER SUPPLY A1
FINISH WAVETEK PROCESS	RELEASE APPROV	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	
	DO NOT SCALE DWG	MODEL NO 158/159 DWG NO 0103-00-0108 REV
	SCALE NONE	CODE IDENT 23338 SHEET 1 OF 1

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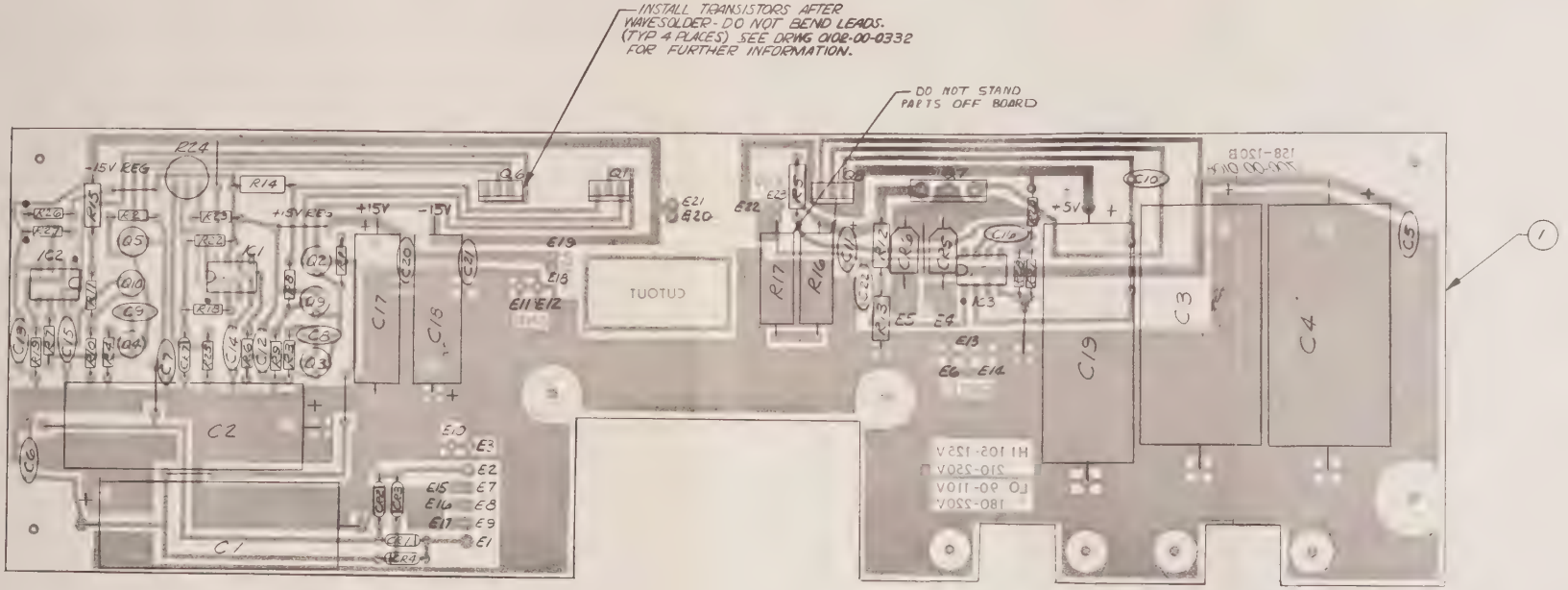
REV	ECN	BY	DATE	APP
C	1069			
D	ECN 1303			
E	ECN 1754	RO		



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	ENGR		TITLE: PC BOARD ASSY POWER SUPPLY BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 158/159	DWG NO 0101-00-0105 REV E
	SCALE -	COST CODE 23338	SHEET 1 OF 1

BRUNING 40-520 15821

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REV	ECN			

REFERENCE DESIGNATORS	PART DESCRIPTION	MFG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DWG, POWER	0101-00-0108	WVTK	0101-00-0108	1
NONE	SCHEMATIC, POWER	0103-00-0108	WVTK	0103-00-0108	1
C6 C7	CAP,CER,.01MF,50V	CK-103	CML	1500-01-0310	2
C12 C13 C14 C15 C20 C21 C22 C5	CAP,CER,.1MF,20V	UK20-104	CML	1500-01-0413	8
C10 C8 C9	CAP,CER,33PF,1KV	DD-330	AMCO	1500-03-3011	3
C16	CAP,CER,47PF,1KV	DD-470	AMCO	1500-04-7011	1
C1 C2	CAP,ELECT,1000MF,35V	39D108G035GL6	SPRAG	1500-31-0212	2
C19	CAP,ELECT,1900MF,15V	39D198G015GL4	SPRAG	1500-31-9201	1
C17 C18	CAP,ELECT,250MF,10V	500D257G010DF7	SPRAG	1500-32-5101	2
C3 C4	CAP,ELECT,4000MF,15V	39D408G015JL4	SPRAG	1500-34-0201	2
C11	CAP,TANT,.22MF,15V	196D224X9015KA1	SPRAG	1500-72-2001	1
I	POWER	15A-120	WVTK	1700-00-0108	1
R24	PUT,1K1M,1%	S1AK1K	BECK	0600-01-0209	1
R14 R15	RES,C,1/2W,5%,3.9	RC20GF-3R9	STKPL	4700-25-0399	2
R5	RES,C,1/2W,5%,620	RC20GF-621	STKPL	4700-25-6200	1
R6 R7	RES,MF,1/8W,1%,2.21K	MA55D-2211F	IRC	4701-03-2211	2
R22	RES,MF,1/8W,1%,2.87K	MA55D-2871F	IRC	4701-03-2871	1

WAVETEK PARTS LIST	TITLE POWER	ASSEMBLY NO. 1100-00-0108	REV F
		PAGE: 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	MFG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q2 Q3 Q9	TRANS	2N3646	NSC	4901-03-6460	3
Q10 Q4 Q5	TRANS	2N2219	FAIR	4901-04-2480	3
Q1	TRANS	TIP-29	TI	4902-00-0290	1
Q6 Q8	TRANS	TIP-30	TI	4902-00-0300	2
Q7	TRANS	TIP-35	TI	4902-00-0350	1
IC3	IC	LM376	NSC	7000-03-7600	1
IC1 IC2	IC	MA-741	FAIR	7000-07-4100	2

WAVETEK PARTS LIST	TITLE POWER	ASSEMBLY NO. 1100-00-0108	REV F
		PAGE: 3	

REFERENCE DESIGNATORS	PART DESCRIPTION	MFG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R21	RES,MF,1/8W,1%,3.32K	MA55D-3321F	IRC	4701-03-3321	1
R18	RES,MF,1/8W,1%,3.92K	MA55D-3921F	IRC	4701-03-3921	1
R3 R4	RES,MF,1/8W,1%,464	MA55D-4640F	IRC	4701-03-4640	2
R1 R19 R2	RES,MF,1/8W,1%,4.75K	MA55D-4751F	IRC	4701-03-4751	3
R20	RES,MF,1/8W,1%,5.76K	MA55D-5761F	IRC	4701-03-5761	1
R25	RES,MF,1/8W,1%,6.19K	MA55D-6191F	IRC	4701-03-6191	1
R28	RES,MF,1/8W,1%,69.8K	MA55D-6982F	IRC	4701-03-6982	1
R11 R8	RES,MF,1/8W,1%,825	MA55D-8250F	IRC	4701-03-8250	2
R23	RES,MF,1/8W,1%,8.25K	MA55D-8251F	IRC	4701-03-8251	1
R10 R9	RES,MF,1/8W,1%,9.09K	MA55D-9091F	IRC	4701-03-9091	2
R13	RES,MF,1/4W,1%,332	MA60D-3320F	IRC	4701-13-3320	1
R12	RES,MF,1/4W,1%,49.9	MA60D-49R9F	IRC	4701-13-4990	1
R16 R17	RES,WW,5W,10Ω,.1	CP-5	DALE	4702-66-0019	2
R26 R27	RES,SEL,2-10K,1/8W 2PT:2W(1)-05-1 VC	142-501-64A	WVTK	4789-00-0019	1
CR7	DIODE	1N4581	MILNO	4801-01-4581	1
CR1 CR2 CR3 CR4	DIODE	SCE-1	SEMT	4801-02-0001	4
CR5 CR6	DIODE	6081	IR	4806-02-0060	2

WAVETEK PARTS LIST	TITLE POWER	ASSEMBLY NO. 1100-00-0108	REV F
		PAGE: 2	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PARTS LIST POWER SUPPLY ASSY
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ± 1°		
	DO NOT SCALE DWG		MODEL NO 159 / DWG NO 1100-00-0108 / REV F
	SCALE		CODE IDENT 23338 / SHEET 1 OF

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-5894

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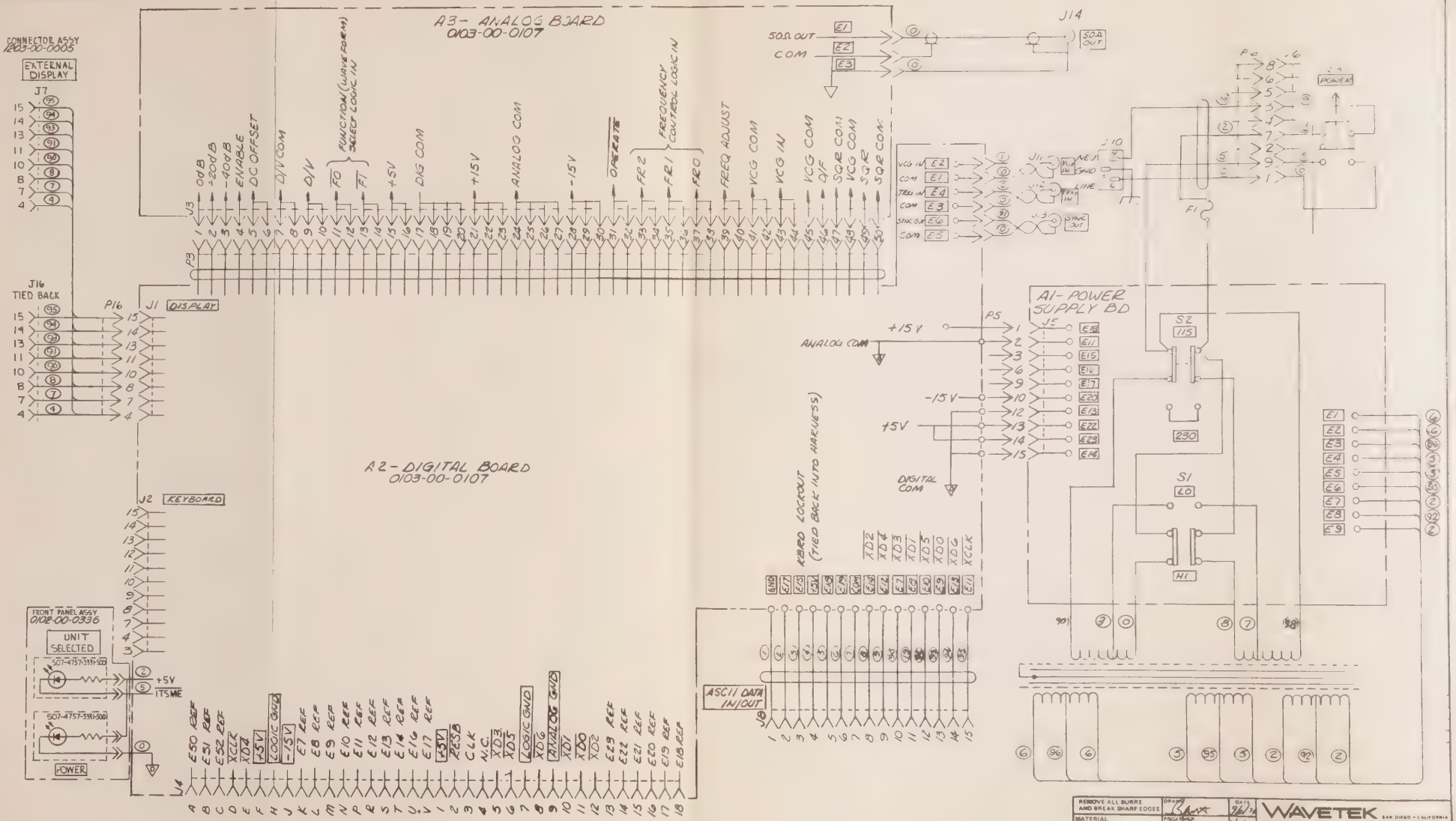
REV	ECN	BY	DATE	APP
A	ECN 3288	RO	4.7	



NOTES:
1. ▭ DENOTES ACTUAL LABELING ON UNIT
2. BAR OVER MNEMONIC DENOTES TRUE WHEN LOW
3. ○ DENOTES WIRE COLOR PER RESISTOR CODE

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE 9/6/84	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENG	9/6/84	TITLE: INTERCONNECT DIAGRAM 158 OPTION
	RELEASE APPROV	10/1/84	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO 158/159
	SCALE		DWG NO 0004-00-0086 REV A
			CODE IDENT 23338 SHEET 1 OF 2

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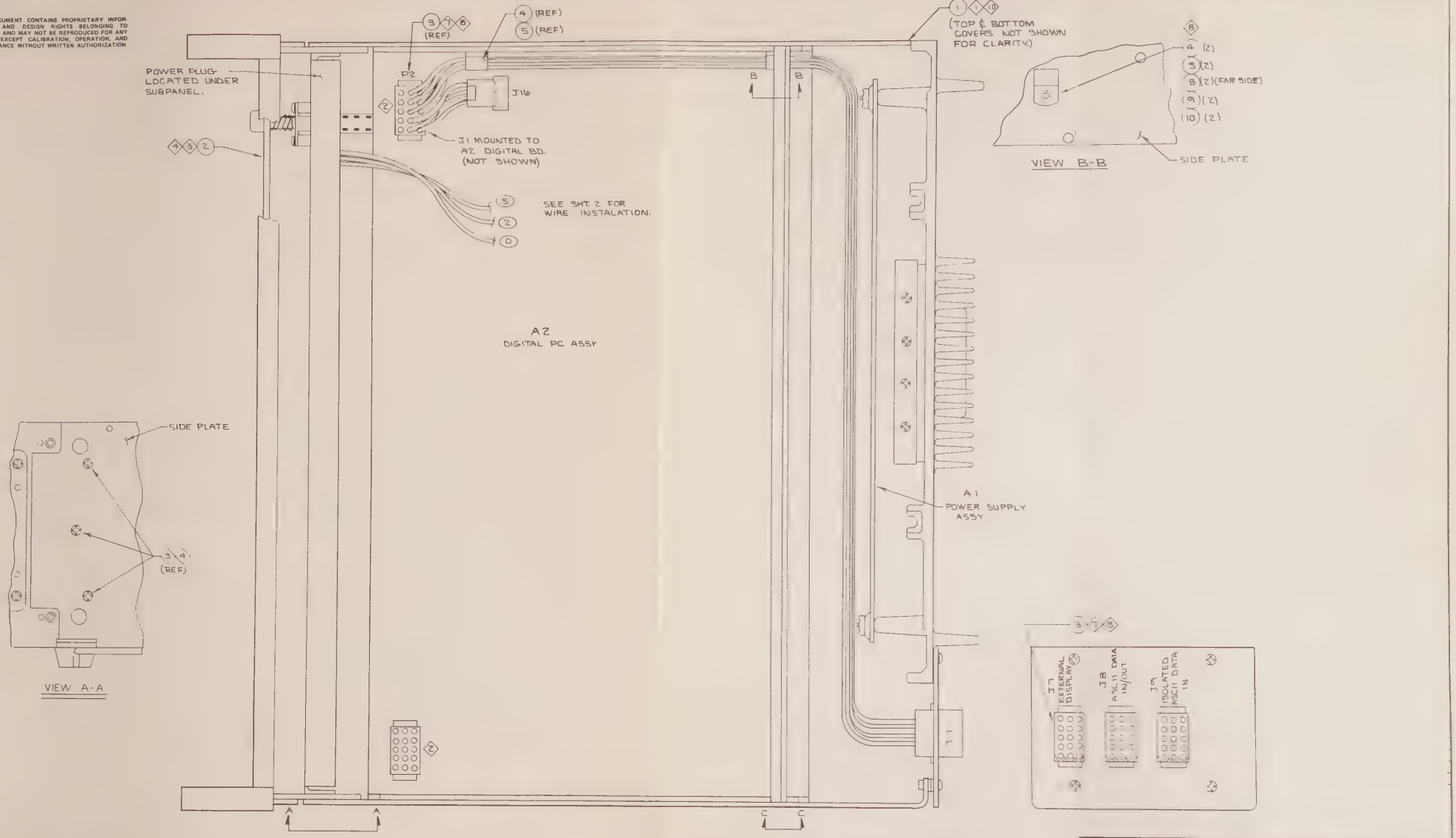
REV	ECN	BY	DATE	APP



(3) PULL HARDWARE FOR FIELD INSTALATION ONLY.

2. ◇ DENOTES LINE NUMBER FOR MODIFCATION PROCEDURE.

NOTE UNLESS OTHERWISE SPECIFIED 1 ○ DENOTES WIRE COLOR PER RESISTOR CODE.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN ADKINS	DATE 10-2-78
MATERIAL	ENGR	
	RELEASE APPROV ZB 12/14/4	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 010 ANGLES ± 1° XX ± .005	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: MODIFICATION DWG 158 OPTION

MODEL NO	DWG NO	REV
158	010200-0303	

CODE IDENT 23338 SHEET 1 OF 3

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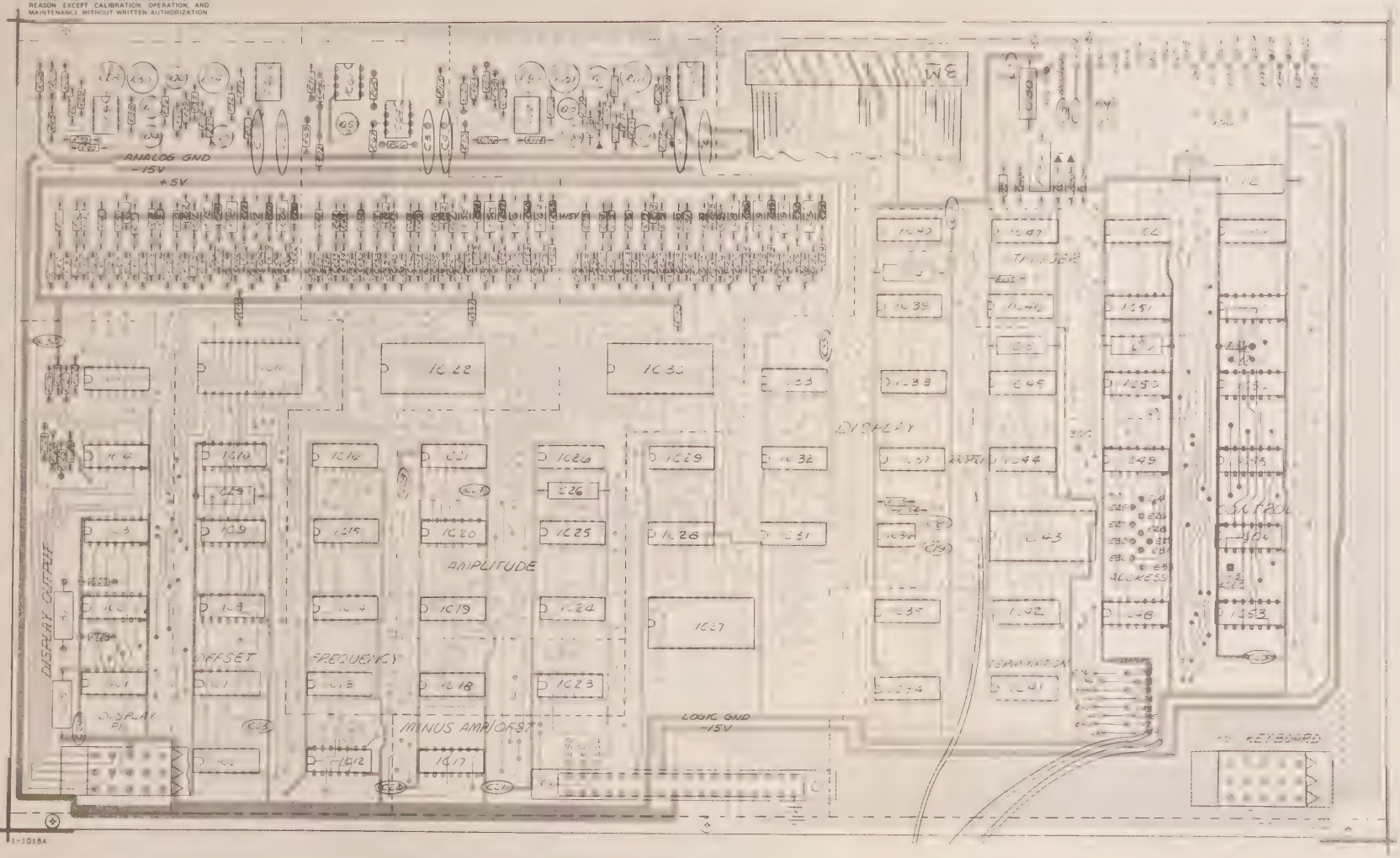

1-1018A

2. ○ DENOTES WIRE COLOR PER RESISTOR CODE

1. ALL DIODES ARE POSITIONED AS SHOWN

NOTE UNLESS OTHERWISE SPECIFIED

SHEET 3 OF 3 IS "A" SIZE MOD. PROC.

REMOVE ALL BURRS AND SHARP EDGES

FINISH WAVETEK PROCESS

DRAWN

RELEASE APPROV 2PS 12/2/14

TOLERANCE UNLESS OTHERWISE SPECIFIED
.*** .010 ANGLES 1
.** .020

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE MODIFICATION DWG 158 OPTION

MODEL NO 158

DWG NO 0102-00-0303

REV

CODE IDENT 23338

SHEET 2 OF 3

MODIFICATION PROCEDURE

1. REMOVE TOP AND BOTTOM COVERS.

2. DISCONNECT POWER PLUG P6, DISPLAY PLUG P1 AND KEYBOARD PLUG P2.

3. REMOVE FRONT PANEL ASSY 1100-00-0075 AND RETURN TO STOCK.

4. INSTALL FRONT PANEL ASSY 1101-00-0078 AS SHOWN.

5. CONNECT POWER PLUG P6, TO NEW FRONT PANEL ASSY.

6. REMOVE SCREWS AND RAISE ANALOG BOARD TO FACILITATE INSTALLATION OF WIRES TO DIGITAL BOARD.

7. REMOVE BLANK MOLEX CONNECTOR FROM THE EXTERNAL DISPLAY LOCATION ON REAR PANEL AND RETURN TO STOCK.

8. INSTALL CONNECTOR ASSY 1203-00-0005. CONNECT P16 TO J1 ON THE A2 DIGITAL PC ASSY. INSTALL MOLEX TO EXTERNAL DISPLAY LOCATED ON THE REAR EXTENDER AS SHOWN.

9. LOWER ANALOG PC ASSY AND INSTALL SCREWS.

10. INSTALL TOP AND BOTTOM COVERS.

DWG NO.	REV
0102-00-0303	

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	DWG=MFGR=PART=NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG. 158 MOD	0102-00-0303	WVTK	0102-00-0303	1
3	CABLE ASST	158-039	WVTK	1203-00-0005	1
NONE	CABLE CLAMP	835	SMITH	2800-00-0010	2
NONE	RETAINER,SPRING	U-193	WEKSK	2800-09-0007	2

WAVETEK PARTS LIST

TITLE
MODIFICATION KIT

ASSEMBLY NO
1101-00-0044

REV
A

PAGE: 1

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROVENOR	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
MODIFICATION, 158

MODEL NO	DWG NO	REV
158	1101-00-0044	A

CODE IDENT 23338 SHEET 1 OF 1

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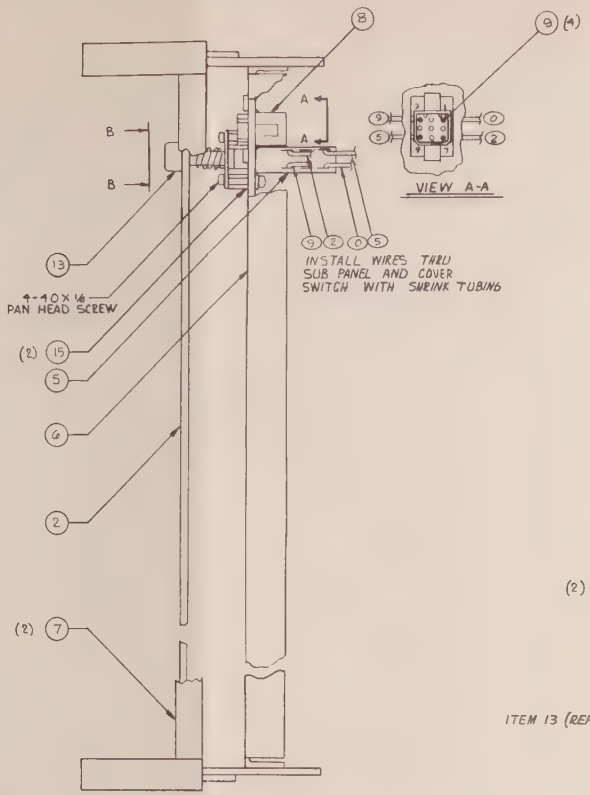
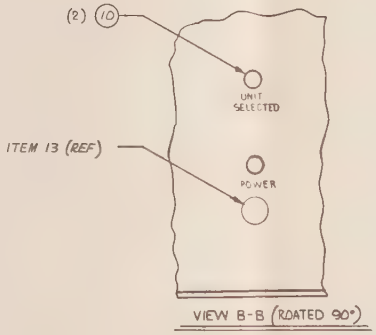
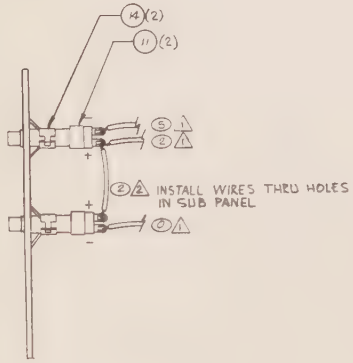
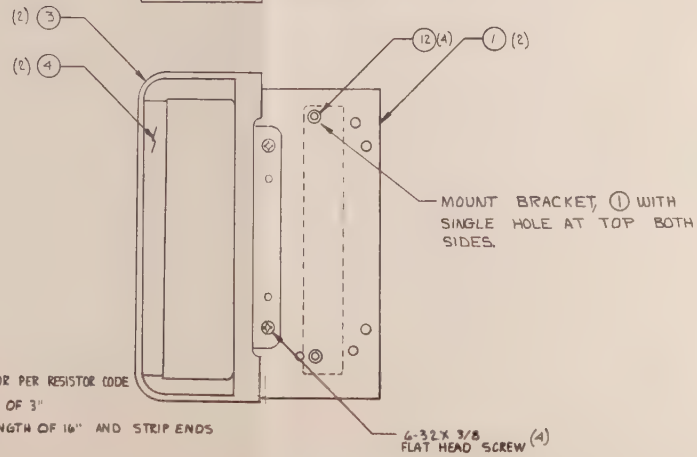
REV	ECN	BY	DATE	APP
A	ECN 20	RJ	4/16	
B	ECN 1315	[illegible]	6/15	









3. ◯ DENOTES WIRE COLOR PER RESISTOR CODE

2 CUT WIRE TO A LENGTH OF 3"

1 CUT WIRES TO A LENGTH OF 16" AND STRIP ENDS

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BARNETT	DATE 9/6	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJECT ENG [illegible]	10/6/14	TITLE FRONT PANEL ASSY- 158 OPTION
FINISH WAVETEK PROCESS	RELEASE APPROV [illegible]		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO 159	DWG NO 0102-00-0336 REV B
	SCALE FULL	CODE IDENT 23338	SHEET 1 OF 1

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REV	ECN	BY	APP	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY UNBG, FT PNL	0102-00-0336	WVTK	0102-00-0336	1
6	PANEL,SUB	158-323	WVTK	1400-00-0723	1
1 1A	BRKT	158-324	WVTK	1400-00-0733	2
15 15A	STANDOFF	013-003-2	WVTK	1400-00-2503	2
3 3A	HANDLE,A/A FRUM[NEO-00-3581	147-304	WVTK	1400-00-3589	1
4 4A	TRIM,HANDLE REF:3200-00-0006	147-305	WVTK	1400-00-3619	2
2	PANEL,FT	158-326	WVTK	1400-00-5570	1
7	TRIM REF:3201-00-0005	1400-00-7019	WVTK	1400-00-7019	1
8	PLUG,9PIN	03-00-2091	MOLEX	2100-02-0011	1
11 11A	CONN,LAMP	515-0674	DILCO	2100-03-0024	2
NONE	PIN,MALE	02-00-2103	MOLEX	2100-05-0003	4
NONE	LAMP CANTRIDGE	507-4757-3331-500	DILCO	2400-02-0016	2
14 14A	CLIP	515-0051	DILCO	2800-36-0003	2
5	SWITCH ASSY PB	157-422	WVTK	5103-00-0011	1
13	BUTTON	J-52305-BLACK	CML	5103-04-0003	1

WAVETEK PARTS LIST	TITLE FT PANEL ASSY	ASSEMBLY NO. 1101-00-0078 SHEET 1	REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE FRONT PANEL ASSY
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		MODEL NO 158 DWG NO 1101-00-0078 REV B
	DO NOT SCALE DWG		CODE IDENT 23338 SHEET 1 OF 1
	SCALE		

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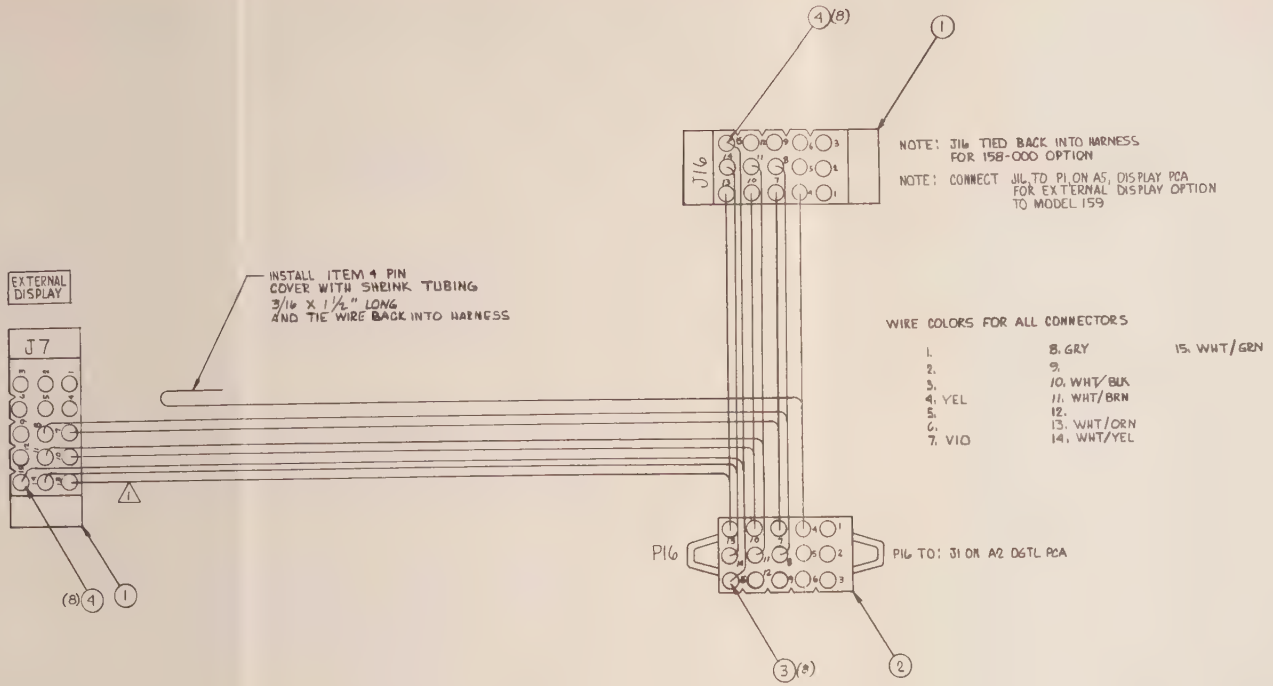
REV	ECN	BY	DATE	APP



3. TIE WIRES USING SMALL CABLE TIE 23M AS REQ.

⚠2 CUT WIRES TO A LENGTH OF 3.0 INCHES

⚠1 CUT WIRES TO A LENGTH OF 28.5 INCHES

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: Ramsett	DATE: 9/0	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR: [illegible]	10/9/4	TITLE: CONNECTOR ASSY- EXT DISPLAY
FINISH: WAVETEK PROCESS	RELEASE APPROV: [illegible]	11/1/4	
	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO: 158/159 DWG NO: 1203-00-0005 REV:
	SCALE		CODE IDENT: 23338 SHEET 2 OF 2

Option 159-005 (General Purpose Interface Bus) is designed to be compatible with IEEE Standard 488-1975. Previous names, including IEC and HPIB, always refer to the GPIB.

GPIB Option

The GPIB Option 159-005 implements Acceptor Handshake (AH), Listen (L), Remote Enable (REN) and Go To Local (GTL). Group Execute Trigger (GET) is not implemented. No provisions for Service Request or Polling have been made. (The SRQ and EOI lines are not used.)

REN Function

The GPIB equipped generator will be in a Remote Only condition if the GPIB option card is addressed to Listen while the REN line is set. (Remote Only implies that the generator's keyboard will be disabled.) Either a Go To Local (GTL) command or resetting the REN line will enable the generator's keyboard.

GPIB Listen Address

The GPIB Listen Address is independent of the generator Unit Address. The GPIB option is a translator for up to nine Wavetek generators. The ASCII G1 thru G9 selects individual generators via the translator.

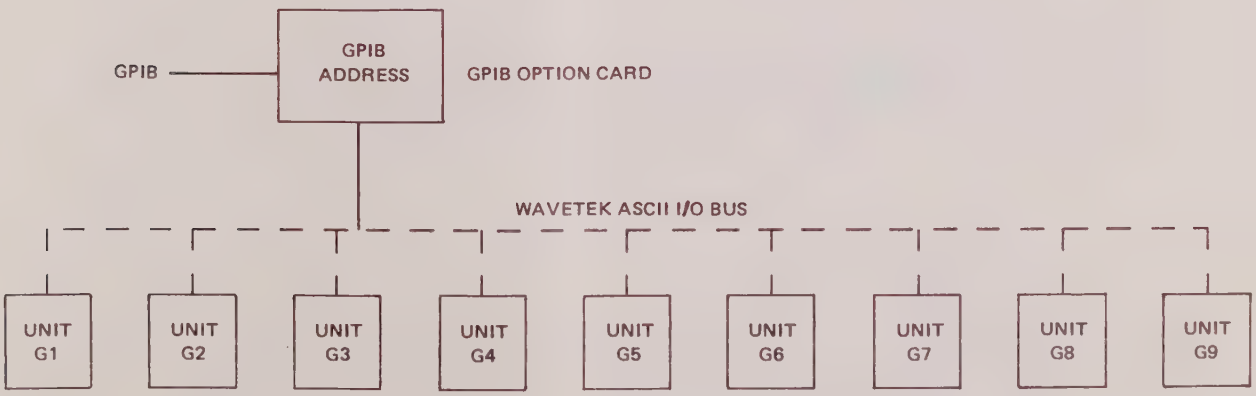
NOTE

The GPIB address enables only the translator.

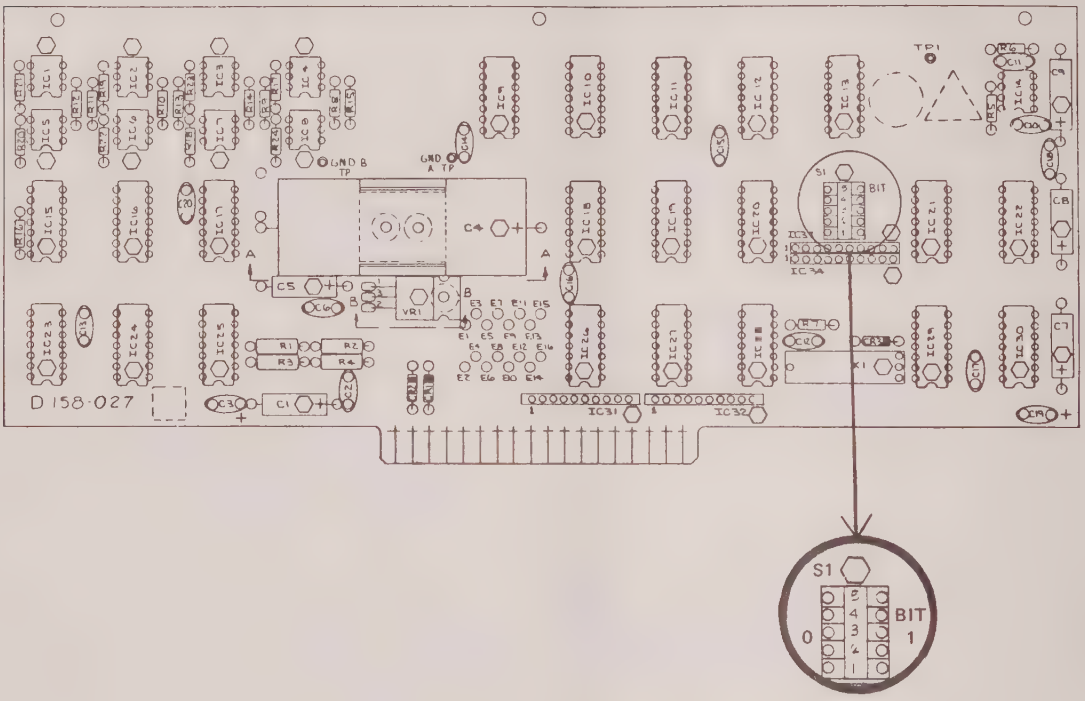
Unless otherwise specified, GPIB options are delivered with an address of > for the HP9830 (device 30 for HP9825/ Tektronix 4051). This address can be changed by switch S1 on the GPIB option card.

Changing GPIB Address

Remove top cover of 158/159. Locate vertically mounted option card at front of generator. Remove screws at both ends of mounting bar; remove card.



Wavetek Generators/Unit Addresses



Example: Listen Address of $ (device 4)

DI0 (switch section) Lines

	S1		
DI05 = 0	X	5	
DI04 = 0	X	4	
DI03 = 1		3	X
DI02 = 0	X	2	
DI01 = 0	X	1	

(1 = open switch)

Figure A-1. GPIB Option Card

The five sections of switch S1 (figure A-1) correspond to the lower 5 Data I/O lines of the GPIB: switch section 1 = DI01, section 2 = DI02, etc. All legal listen addresses are listed in table A-1. Set the switch sections to 0 or 1 as indicated.

Unit Address

Unless otherwise specified, the Models 158 and 159 are delivered with a unit address of 1. This address can be changed by repositioning the address jumper on the digital board of the generator.

Changing Unit Address

Remove top and bottom covers of generator. Remove screws from both ends of the analog board front mounting bar (top horizontal board). Rotate and secure analog board in an UP position. Locate address pads E24 thru E33. (See figure A-2.)

Jumper E29 to E24 for unit address of 1
Jumper E29 to E25 for unit address of 2
Jumper E29 to E26 for unit address of 3
Jumper E29 to E27 for unit address of 4
Jumper E29 to E28 for unit address of 5
Jumper E29 to E30 for unit address of 6
Jumper E29 to E31 for unit address of 7
Jumper E29 to E32 for unit address of 8
Jumper E29 to E33 for unit address of 9

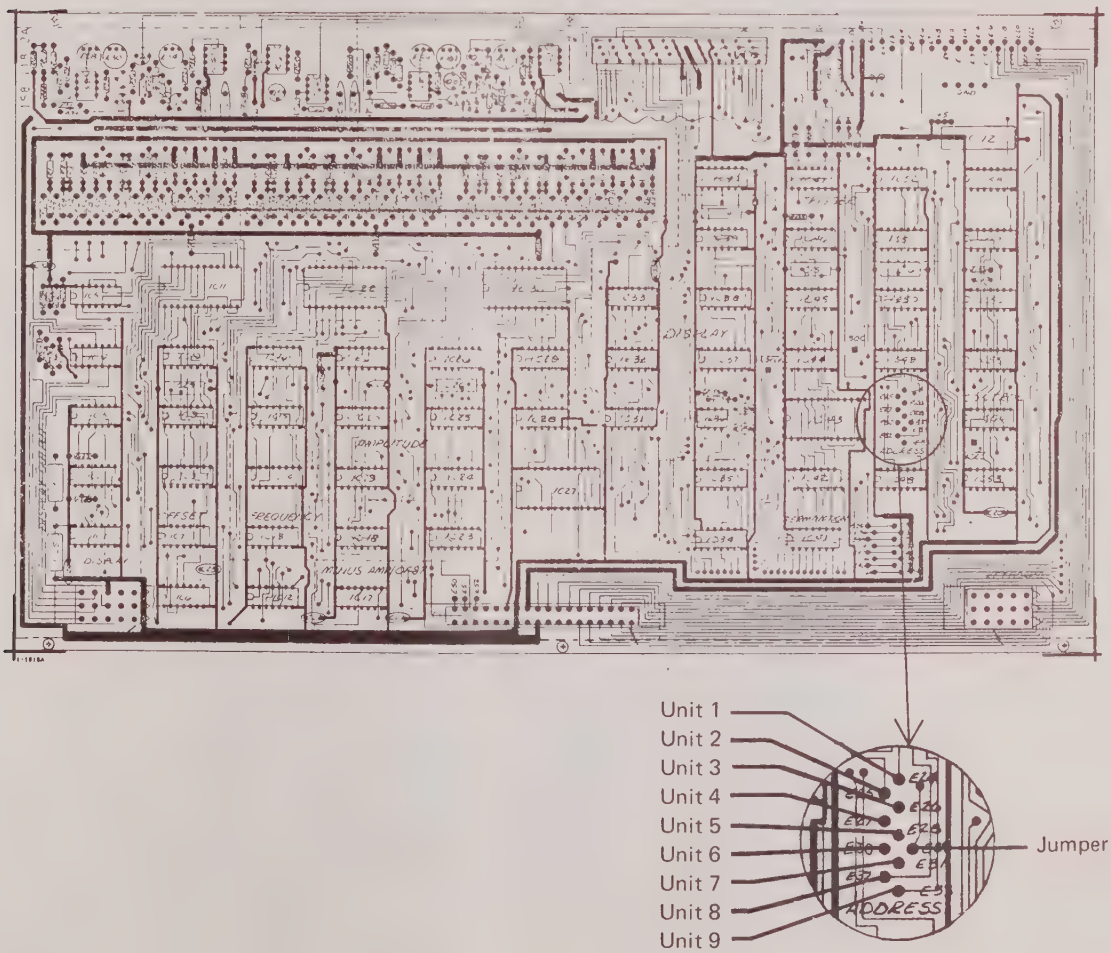


Figure A-2. Model 158/159 Digital Board (Top View)

HP9825 TEK4051	HP9830	Primary Listen Address								
		Decimal Value	DIO Bus							
			8	7	6	5	4	3	2	1
Device Ø	SP	32	0	0	1	0	0	0	0	0
Device 1	!	33	0	0	1	0	0	0	0	1
Device 2	"	34	0	0	1	0	0	0	1	0
Device 3	#	35	0	0	1	0	0	0	1	1
Device 4	$	36	0	0	1	0	0	1	0	0
Device 5	%	37	0	0	1	0	0	1	0	1
Device 6	&	38	0	0	1	0	0	1	1	0
Device 7	'	39	0	0	1	0	0	1	1	1
Device 8	(	4Ø	0	0	1	0	1	0	0	0
Device 9	)	41	0	0	1	0	1	0	0	1
Device 1Ø	*	42	0	0	1	0	1	0	1	0
Device 11	+	43	0	0	1	0	1	0	1	1
Device 12	,	44	0	0	1	0	1	1	0	0
Device 13	-	45	0	0	1	0	1	1	0	1
Device 14	.	46	0	0	1	0	1	1	1	0
Device 15	/	47	0	0	1	0	1	1	1	1
Device 16	0	48	0	0	1	1	0	0	0	0
Device 17	1	49	0	0	1	1	0	0	0	1
Device 18	2	5Ø	0	0	1	1	0	0	1	0
Device 19	3	51	0	0	1	1	0	0	1	1
Device 2Ø	4	52	0	0	1	1	0	1	0	0
Device 21	5	53	0	0	1	1	0	1	0	1
Device 22	6	54	0	0	1	1	0	1	1	0
Device 23	7	55	0	0	1	1	0	1	1	1
Device 24	8	56	0	0	1	1	1	0	0	0
Device 25	9	57	0	0	1	1	1	0	0	1
Device 26	:	58	0	0	1	1	1	0	1	0
Device 27	;	59	0	0	1	1	1	0	1	1
Device 28	<	6Ø	0	0	1	1	1	1	0	0
Device 29	=	61	0	0	1	1	1	1	0	1
Device 3Ø	>	62	0	0	1	1	1	1	1	0
Unlisten	?	63	0	0	1	1	1	1	1	1
						5	4	3	2	1
						Switch Sections				

NOTE: Unlisten (?) cannot be used as an address.

Table A-1. General Purpose Interface Bus Addresses

PROGRAMMING THE MODEL 158-159 EQUIPPED WITH THE IEEE 488 OPTION

```
100  REM PROGRAM DEMONSTRATES USE OF WAVETEK MODEL 158-159 GENERATOR
110  REM ASSUMES MODEL 30 CALCULATOR WITH EXTENDED I/O
120  REM 9820 AND 21 CALCULATORS USE FORMAT B AND WBYTE CMD COMMANDS
130  REM
140  REM UNIT IS ADDRESSED BY A CMD "?U>", "G1"
150  CMD "?U>", "G1"
160  REM WHERE THE FIRST GROUP SELECTS H/P BUS (UNIT 13) UNLISTENS (?),
170  REM THEN SELECTS CALCULATOR TO BE TALKER, > IS ADDRESSED AS A LISTENER
180  REM SECOND GROUP SELECTS UNIT 1 ATN IS SET FOR FIRST GROUP, RESET FOR SECOND
190  REM A1 IS THE UNIT NUMBER; 13 FOR H-P INTERFACE BUS
200  A1=13
210  REM
220  REM AMPLITUDE MAY BE DRIVEN BY;
230  A=5
240  OUTPUT (A1, 250)A;
250  FORMAT "A", E9.2
260  REM   SEMICOLON INHIBITS CR, LF.
270  REM
280  REM FREQUENCY MAY BE DRIVEN BY;
290  F=1234567
300  OUTPUT (A1,310)F;
305  REM USE OF 1000 FORMAT SPECIFICATION DELETES LEADING BLANKS
310  FORMAT "F",E1000.2
320  REM
330  REM OFFSET MAY BE DRIVEN BY;
340  O=1
350  OUTPUT (A1,360)O;
360  FORMAT "D",F6.2
370  REM NOTE THAT OFFSET DOES NOT HAVE A MULTIPLIER DIGIT
380  REM
390  REM FUNCTION AND MODE ARE DRIVEN BY;
400  OUTPUT (A1,*)"B0 C0";
410  REM WOULD SELECT MODE (B) 0, CONTINUOUS, FUNCTION (C) 0 SIN. .
420  REM LEGAL MODE VALUES ARE 0,1,2: FUNCTION INCLUDES 0,1,2,3. .
430  REM OUTPUT IS ENABLED BY;
440  OUTPUT (A1,*)"H"
450  REM WHERE H ENABLES OUTPUT OF GENERATOR TO CONNECTOR. . .
460  REM SENDING AN "I" WILL DISCONNECT GENERATOR OUTPUT.
470  REM
480  REM SPECIAL CHARACTERS CONTROL H-P INTERFACE BUS. . .
490  REM ATN IS ENABLED BY OUTPUT (13,500)256;
500  FORMAT B
510  REM ATN IS RESET BY OUTPUT (13,500)512;
520  REM THESE COMMANDS MAY BE CONCATENATED TO GENERATE UNIVERSAL COMMANDS
530  OUTPUT (A1,500)256,1,512;
540  REM WILL SET ATN, OUTPUT A GO TO LOCAL CHARACTER 'GTL=01', THEN TURN ATN OFF
550  REM
560  OUTPUT (A1,500)768;
570  REM WILL ASSERT THE REN LINE TO ENABLE INSTRUMENTS IN THE REMOTE MODE
580  REM ****NOTE INSTRUMENT WILL NOT GO REMOTE UNTIL ADDRESSED. .
590  REM UNIT WILL STAY REMOTE UNTIL A 'GTL' OR REN IS RESET. .
600  REM  UNLISTEN ALL DEVICES
610  CMD "?"
620  REM REN IS RESET BY;
630  OUTPUT (A1,500)1024;
640  DISP "END TEST";
650  STOP
660  REM
670  REM ************************************************************************************
680  REM
690  REM  SAMPLE PROGRAM
700  A=0
710  F=123456
720  O=M=U=0
730  REM MODE=FUNCTION=0=CONTINUOUS, SIN WAVE. . .
740  REM ADDRESSES THE UNIT ON THE H-P INTERFACE BUS WITH REN ENABLED
750  OUTPUT (13,500)768
760  CMD "?U>"
770  OUTPUT (13,780)A,F,O,U,M;
780  FORMAT "G1A",E9.2,"F",E9.2,"D",F6.2,"B",F4.0,"C",F4.0,"HA"
790  REM LAST A DISPLAYS AMPLITUDE ON MODEL 159 DISPLAY. . .
800  FOR L=1 TO 100
810  OUTPUT (13,820)A;
820  FORMAT "A",E1000.2
830  A=9.99*RND(5)
840  DISP L
850  NEXT L
860  REM SENDS GTL TO ADDRESSED UNIT ONLY TO ENABLE KEYBOARD. . .
870  OUTPUT (13,500)256,1,512;
880  REM REN IS STILL ASSERTED.
890  DISP "STOP ** CONT-EXE TO REPEAT";
900  CMD "?"
910  STOP
920  GOTO 700
930  REM NOTE STOP BUTTON WILL ISSUE EOP-ICL INTRFC CLEAR WHICH WILL SEND
940  REM 159 TO LOCAL MODE. . . .
950  REM
960  REM ************************************************************************************
970  REM
980  END
```

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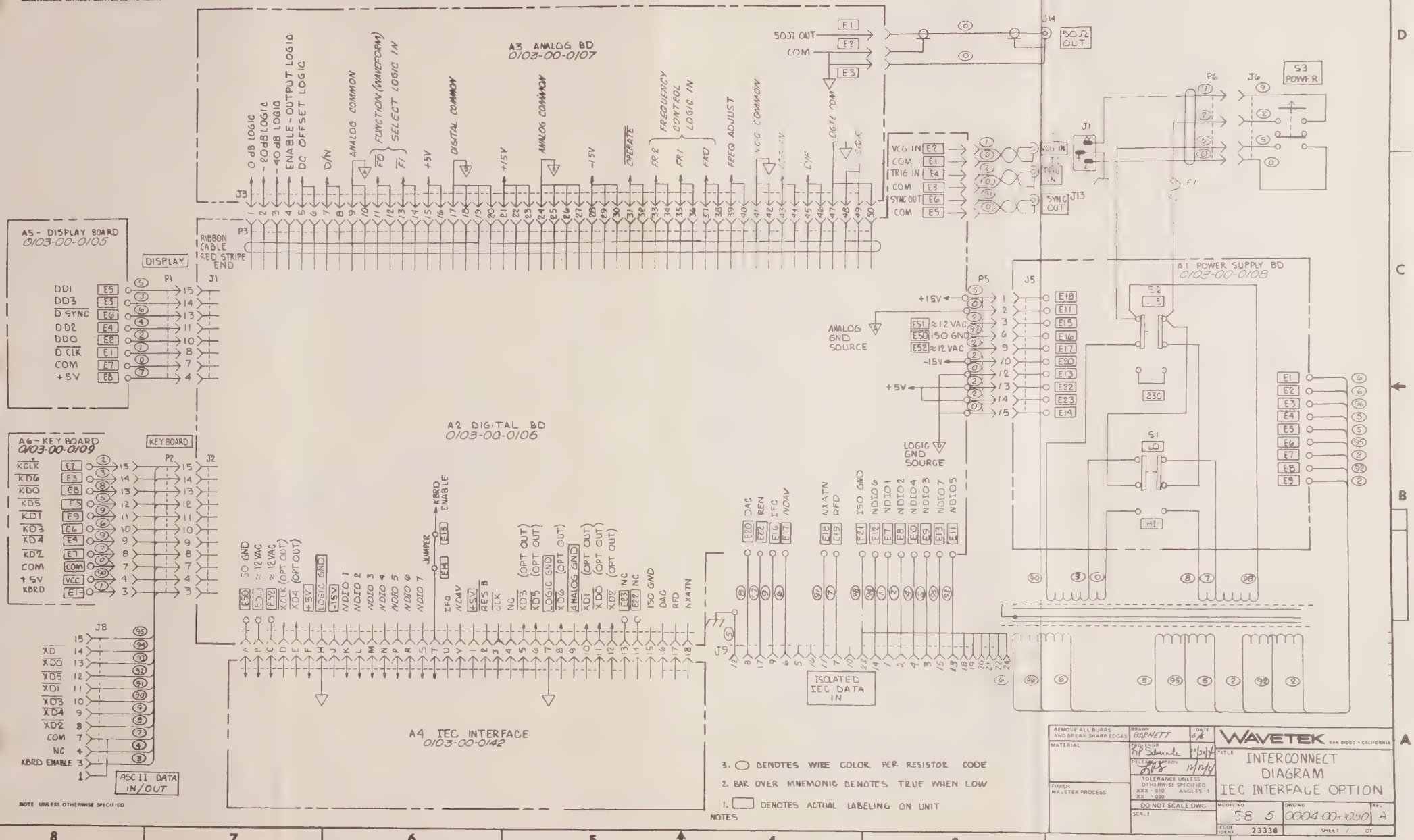
REV	ECN	BY	DATE	APP
A	ECN 1368	RO	11-17-75	

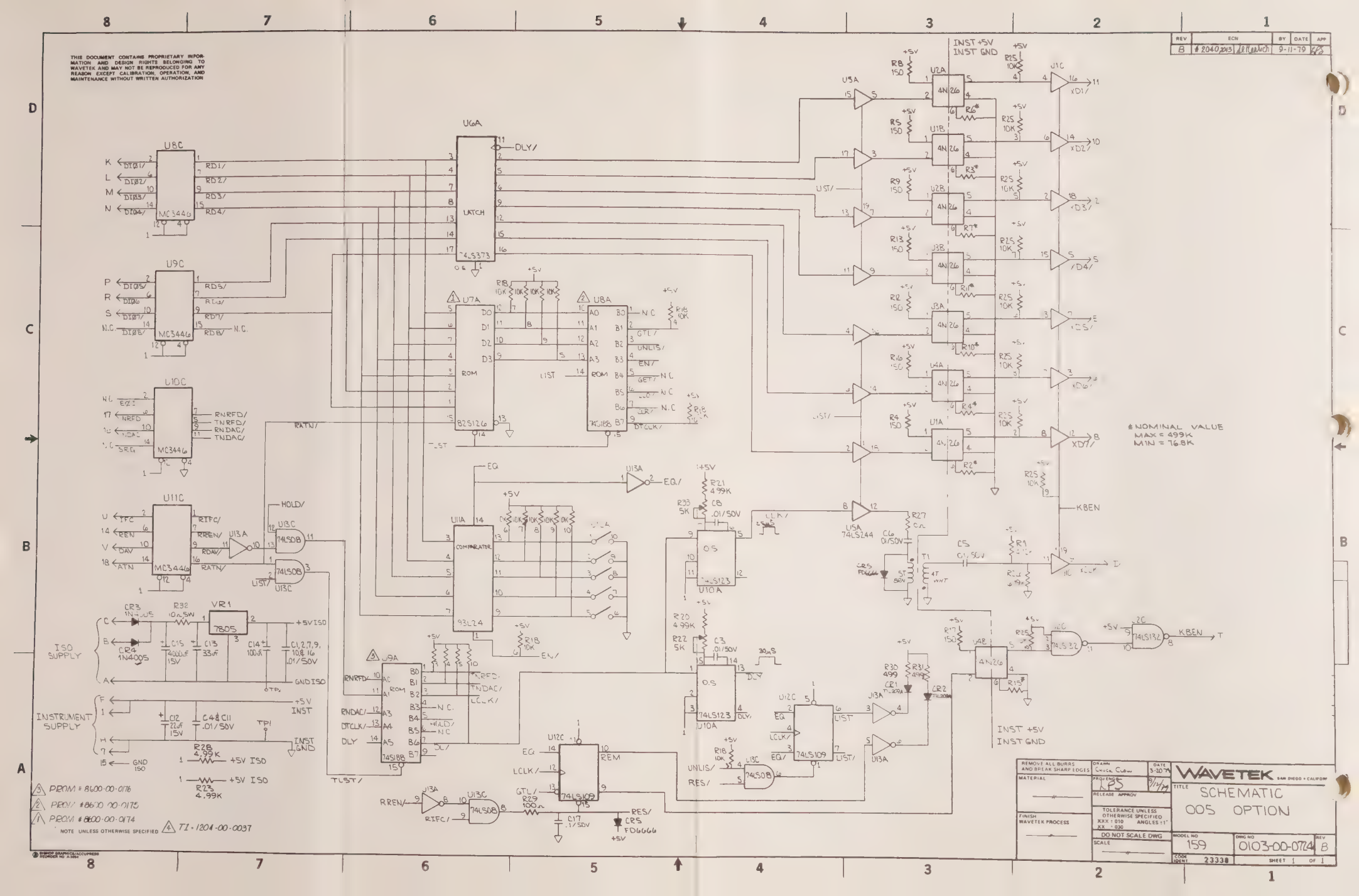


NOTES

1. ☐ DENOTES ACTUAL LABELING ON UNIT
2. BAR OVER MNEMONIC DENOTES TRUE WHEN LOW
3. ○ DENOTES WIRE COLOR PER RESISTOR CODE

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BARNETT	DATE 6/8	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	ENGINEER		TITLE INTERCONNECT DIAGRAM IEC INTERFACE OPTION
FINISH WAVETEK PROCESS	RELEASED APPROV		TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - 010 ANGLES - 1 XX - 030
DO NOT SCALE DWG	SCALE		MODEL NO 58 5 DWG NO 0004-00-0350 REV A
			CODE IDENT 23330 SHEET / OF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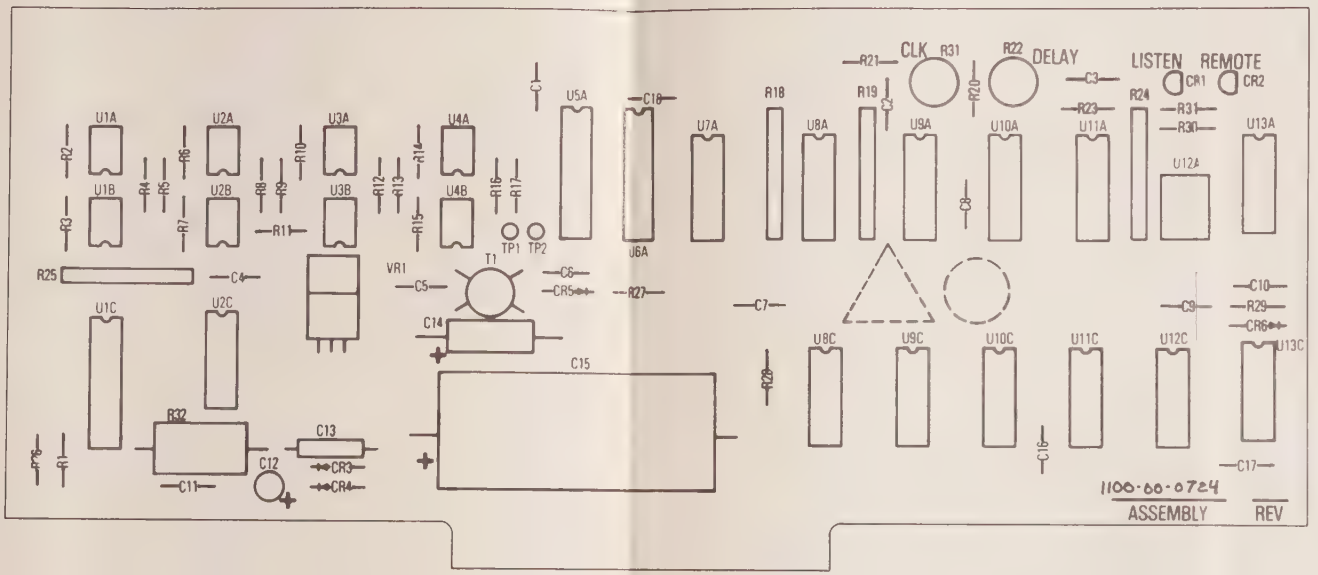
REV B ECN # 2040 2013 BY RMcGRAW DATE 9-11-79 APP
INST +5V
INST GND
U8C
U9C
U10C
U11C
MC3446
U6A
LATCH
74LS373
U7A
ROM
82S126
U8A
74LS188
U10A
COMPARATOR
93L24
U9A
U11A
U12C
74LS109
U13A
U13C
74LS08
U10A
74LS123
U12A
U13A
74LS86
U5A
74LS244
U1A
U2A
U3A
U4A
U1B
U2B
U3B
U4B
U1C
U2C
U3C
U4C
4N26
VR1
7805
ISO SUPPLY
INSTRUMENT SUPPLY
+5VISO
GNDISO
+5V INST
INST GND
+5V ISO
GND ISO
R28 4.99K
R23 4.99K
R21 499K
R22 5K
R33 5K
R20 499K
R30 499
R31 499
R27 OPEN
R1 OPEN
* NOMINAL VALUE MAX = 499K MIN = 76.8K
DLY/
LIST/
UST/
EQ/
HOLD/
RATN/
TLST/
KBEN
XD1/
XD2/
XD3/
XD4/
XD5/
XD6/
XD7/
XD8/
RNRFD/
TNRFD/
RNDAC/
TNDAC/
LCLK/
DTCLK/
RREN/
RIFC/
REM
GTL/
RES/
UNLIS/
CR1 TIL209A
CR2 TIL209A
CR3 1N4005
CR4 1N4005
CR5 FD6666
T1 4T WHT
ROM # 8600-00-0176
ROM # 8600-00-0175
ROM # 8600-00-0174
NOTE UNLESS OTHERWISE SPECIFIED
TI-1204-00-0037
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN Chuck Clow
DATE 3-20-79
PROJENGR KPS
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 010 ANGLES ± 1° XX ± 030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO CALIFORN
TITLE SCHEMATIC 005 OPTION
MODEL NO 159
DWG NO 0103-00-0174
REV B
CODE IDENT 23330
SHEET 1 OF 1



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN / DATE	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	PROJ ENGR	TITLE: A554 005 OPTION GPIB (IEC) INTERFACE	
FINISH: WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO: 159	DWG NO: 0101-00-0724 REV: B
	SCALE	CODE IDENT: 23338	SHEET 1 OF

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG,IEC OPTION	0101-00-0724	WVTK	0101-00-0724	1
NONE	SCHEMATIC,IEC OPTION	0103-00-0724	WVTK	0103-00-0724	1
T1	TRANSFORMER	1204-00-0037	WVTK	1204-00-0037	1
C1 C10 C16 C18 C2 C3 C4 C5 C6 C7 C8 C9	CAP,CER,MN,.01MF,50V	1801Z5U050A103Z	VRDYN	1500-01-0305	12
C11 C17	CAP,CER,MON,.1MF,50V	1802Z5U050A104Z	VARDN	1500-01-0405	2
C14	CAP,ELECT,100MF,16V	500D107G016DC7	SPRAG	1500-31-0101	1
C15	CAP,ELECT,4000MF,15V	TCG402U015N1L	MAL	1500-34-0211	1
C12	CAP,TANT,22MF,15V	196D226X9015KA1	SPRAG	1500-72-2601	1
C13	CAP,TANT,33MF,10V	150D336X9010B2	SPRAG	1500-73-3601	1
1	IEC INTERFACE	1700-00-0724	WVTK	1700-00-0724	1
5	SKT,IC,16PIN	01LB-16P-108	BUNND	2100-03-0028	5
3	CLAMP	4511-100-68-2C	BEBTM	2800-00-0008	1
4	STANDOFF,SNAGE .125 H,.250 DIA 4-40,.062 MAT'L	95318-0440-5A	AMTOM	2800-03-0004	4
2	HEAT SINK	NR-150A	RCA	2800-11-0002	1
R22 R33	POT,TRIM,5K	91A5K	BECK	4600-05-0205	2
R29	RES,MF,1/8W,1%,100	RN55D-1000F	TRW	4701-03-1000	1

WAVETEK PARTS LIST | TITLE PCA,IEC INTERFACE | ASSEMBLY NO. 1100-00-0724 PAGE: 1 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U13C	IC	74L808	TI	8000-74-0810	1
VR1	VOLTAGE REGULATOR	7805393	FAIR	8000-78-0500	1
U11A	IC	93L24PC	FAIR	8000-93-2410	1
U12C	IC	74LS1098	SIG	8007-41-0910	1
U10A	IC	74LS1238	SIG	8007-41-2310	1
U2C	IC	74LS132	TI	8007-41-3210	1
U1C U5A	IC	74LS244	TI	8007-42-4410	2
U6A	IC	74LS373	MOT	8007-43-7310	1
U7A	IC,PROGRAMMED FMQM18008-21-2601	8600-00-0174	WVTK	8600-00-0174	1
U8A	IC,PROGRAMMED REF18007-41-8800	8600-00-0175	WVTK	8600-00-0175	1
U9A	IC,PROGRAMMED REF18007-41-8800	8600-00-0176	WVTK	8600-00-0176	1

WAVETEK PARTS LIST | TITLE PCA,IEC INTERFACE | ASSEMBLY NO. 1100-00-0724 PAGE: 3 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R27	RES,MF,1/8W,1%,10	RN55D-10R0F	TRW	4701-03-1009	1
R12 R13 R16 R17 R4 R5 R8 R9	RES,MF,1/8W,1%,150	RN55D-1500F	TRW	4701-03-1500	8
R1	RES,MF,1/8W,1%,4.02K	RN55D-4021F	TRW	4701-03-4021	1
R30 R31	RES,MF,1/8,1%,499	RN55D-4990F	TRW	4701-03-4990	2
R20 R21 R23 R28	RES,MF,1/8W,1%,4.99K	RN55D-4991F	TRW	4701-03-4991	4
R26	RES,MF,1/8W,1%,6.19K	RN55D-6191F	TRW	4701-03-6191	1
R10 R11 R14 R15 R2 R3 R6 R7	RES,MF,1/8W,1%,76.8K	RN55D-7682F	TRW	4701-03-7682	8
R32	RES,MM,2W,10%,3.9	8WM 3.9	IHC	4702-45-0399	1
R18 R19 R24 R25	RES MODULE	4310R-101-103	BUNN	4770-00-0008	4
CR3 CR4	DIODE	1N4005	MOT	4806-01-4005	2
CR5 CR6	DIODE	FD-6666	FAIR	4807-02-6666	2
CR1 CR2	LED	TIL-209A	TI	4899-00-0005	2
U12A	SWITCH PC	500-105	DUNCN	5199-00-0001	1
U1A U1B U2A U2B U3A U3B U4A U4B	OPTO-COUPLER	4N26	SPECT	7000-04-2600	8
U10C U11C U8C U9C	IC	MC3446P	MOT	8000-34-4600	4
U13A	IC	74L804	TI	8000-74-0410	1

WAVETEK PARTS LIST | TITLE PCA,IEC INTERFACE | ASSEMBLY NO. 1100-00-0724 PAGE: 2 | REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PARTS LIST IEC (GPIB) INTERFACE PCA
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO 195 / DWG NO 1100-00-0724 / REV
	SCALE		CODE IDENT 23338 / SHEET 1 OF

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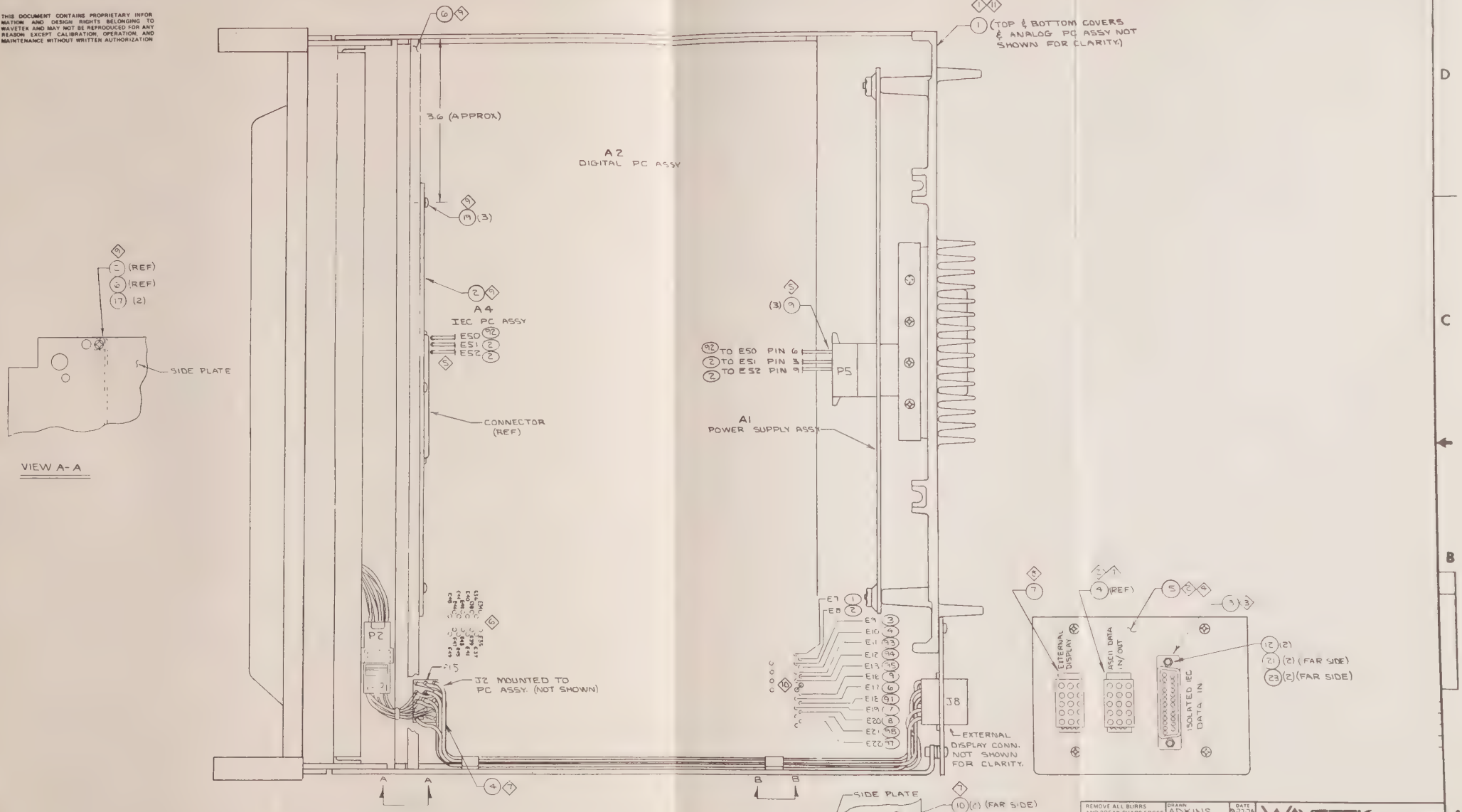
REV	ECN	BY	DATE	APP
1	11			



4. PULL HARDWARE FOR FIELD INSTALLATION ONLY.
3. ◇ DENOTES LINE NUMBER FOR MODIFICATION PROCEDURE. (SEE SHT 2.)
2. PROGRAMING MATING CONNECTORS: IDENTIFY PARTS BY BAG AND TAG AND SHIP WITH INSTRUMENT.
1. ○ DENOTES WIRE COLOR PER RESISTOR CODE.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN ADKINS	DATE 9-7-84	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR LPS	10/1/84	TITLE MODIFICATION DWG IEC OPTION
FINISH WAVETEK PROCESS	RELEASE APPROV LPS		TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES ± 1 .XX ± .030
	DO NOT SCALE DWG		MODEL NO 159
	SCALE 1/1		DWG NO 0102-00-0351 REV
			CODE IDENT 23338 SHEET 1 OF 2

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MODIFICATION PROCEDURE
IEC OPTION

1. REMOVE TOP AND BOTTOM COVERS.
2. REMOVE ASCII DATA IN/OUT MOLEX CONNECTOR J9 FROM EXISTING REAR PANEL EXTENDER P/N 100-00-0710. REMOVE REAR PANEL EXTENDER AND RETURN TO STOCK. UN-SOLDER ALL WIRES THAT GO TO THE A2 DIGITAL PC ASSY, FROM ASCII DATA IN/OUT CONNECTOR J9, AND RETURN THE CONNECTOR ASSY TO STOCK.
3. INSTALL THE IEC CABLE ASSY, P/N 120-00-0002 AND CONNECT WIRES AS SHOWN (REF INTERCONNECT 158-230 J9)
4. INSTALL EXTENDER REAR CASTING P/N 1400-00-5590 AS SHOWN.
5. DISCONNECT THE MOLEX CONNECTOR, P3, FROM THE POWER SUPPLY PC ASSY A1. ATTACH MOLEX PINS P/N 200-05-0026, QTY (3), TO THE ENDS OF THREE WIRES. TWO OF THE WIRES TO BE, 22 AWG, RED, 13.5 INCHES LONG, AND ONE WIRE TO BE 22 AWG, WHT/RED, 13.5 INCHES LONG. INSTALL THE MOLEX PINS AND WIRES INTO P3 AS SHOWN AND SOLDER THE OTHER ENDS TO E50, E51, AND E52. (REF INTERCONNECT 158-_30 P3)
6. REMOVE JUMPERS FROM PADS E34 THRU E49 ON A2 DIGITAL PC ASSY.
7. DISCONNECT KEYBOARD MOLEX P2 FROM J2 AND INSTALL CONNECTOR ASSY, ASCII DATA IN/OUT, P/N 120-00-0003 TO J2. CONNECT THE OTHER END TO THE KEYBOARD MOLEX P2. CONNECT THE OTHER END TO THE KEYBOARD MOLEX P2. INSTALL MOLEX J8, TO ASCII DATA

SH2

DWG NO 0102-00-0351 REV

IN/OUT, LOCATED ON THE REAR PANEL EXTENDER AS SHOWN.

8. INSTALL EMPTY MOLEX CONNECTOR P/N 200-02-0012, IN THE EXTERNAL DISPLAY LOCATION ON THE EXTENDER REAR CASTING P/N 1400-00-5590.
9. INSTALL MTG BAR (OPTION CARD) P/N 400-00-5583, TO PC ASSY IEC, P/N 100-00-0142. AS SHOWN AND PLUG INTO CONNECTOR ON A2 DIGITAL PC BOARD.
   NOTE: IF PHOTO ISOLATION IS NOT REQUIRED INSTALL JUMPERS TO PADS E1 AND E2, E3 AND E4, E5 AND E6, E7 AND E8, E9 AND E10, E11 AND E12, E13 AND E14, E15 AND E16 AS SHOWN ON THE IEC PC ASSY.
10. INSTALL A JUMPER FROM E14 TO E15, ON THE A2 DIGITAL PC ASSY AS SHOWN.
11. INSTALL TOP AND BOTTOM COVERS.

SH3

DWG NO 0102-00-0351 REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN
DATE 5-10-79
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
MODIFICATION
IEC OPTION

MODEL NO 159
DWG NO 0102-00-0351
REV
CODE IDENT 23338
SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A1884

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	UNIG-MFGR-PART-NO	MFGR	MANUFR NO.	QTY/PI
NONE	ASSY UNGR, IEC MOD	0102-00-0351	AVTA	0102-00-0351	1
3	CABLE ASSY	150-033	AVTA	1207-00-0004	1
4	CABLE ASSY	150-055	AVTA	1207-00-0005	1
6	BAR,SUPT	150-350	AVTA	1400-00-5505	1
5	EXT,CABLING	150-353	AVTA	1400-00-5500	1
7	CONN,15PIN	03-09-1151	MOLEX	2100-02-0012	1
8	PLUG,15PIN	03-09-2151	MOLEX	2100-02-0013	1
NONE	PIN,MALE	02-09-2110	MOLEX	2100-03-0005	10
10	CABLE CLAMP	035	SMITH	2000-00-0010	2
11 11A	RETAINER,SPRING	0-191	AEROX	2800-09-0007	2
12 12A	JACK SCREW	408-10E475	AMPH	2200-23-0008	2

WAVETEK PARTS LIST	TITLE MODIFICATION KIT	ASSEMBLY NO. 1101-00-0229 PAGE: 1	REV B

NOTE UNLESS OTHERWISE SPECIFIED

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REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PARTS LIST MODIFICATION, IEC (GPIB) OPTION
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO. 159 / DWG NO. 1101-00-0229 / REV B
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

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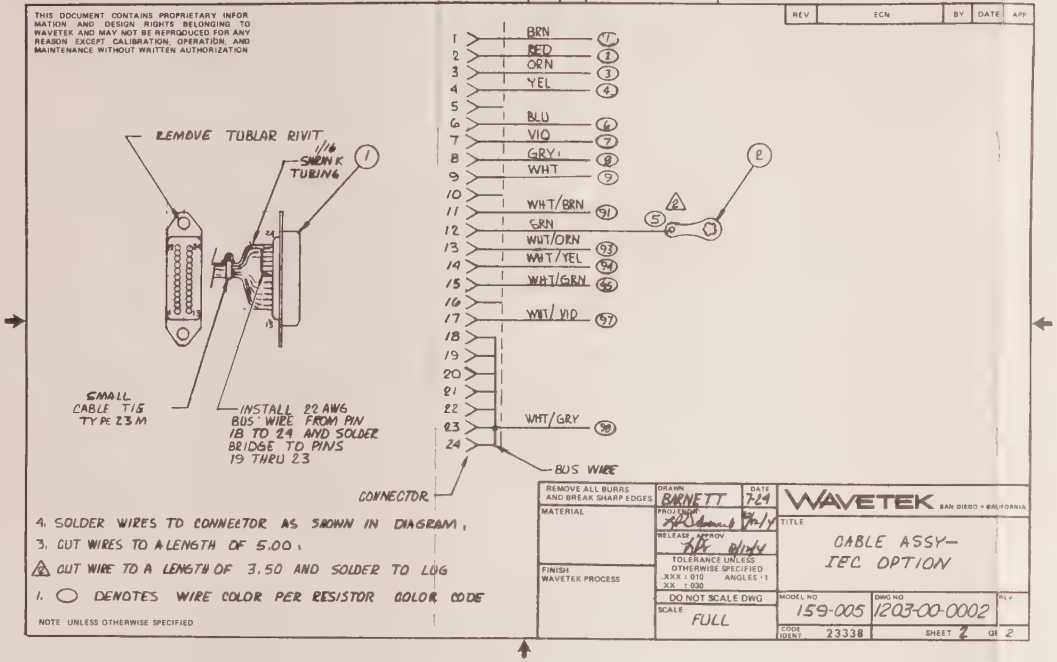

4. SOLDER WIRES TO CONNECTOR AS SHOWN IN DIAGRAM.
3. CUT WIRES TO A LENGTH OF 5.00.
2. CUT WIRE TO A LENGTH OF 3.50 AND SOLDER TO LUG
1. ○ DENOTES WIRE COLOR PER RESISTOR COLOR CODE

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BARNETT	DATE 7-29	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE CABLE ASSY- IEC OPTION
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES ± 1° .XX ± .030		
	DO NOT SCALE DWG		
	SCALE FULL	MODEL NO 159-005	DWG NO 1203-00-0002 REV
		CODE IDENT 23338	SHEET 2 OF 2

REFERENCE DESIGNATORS	PART DESCRIPTION	DWG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	CONN	57-20240	AMPH	2100-02-0060	1
2	TERM,LUCK LUG	1419-6	SMITH	2100-04-0009	1

WAVETEK PARTS LIST	TITLE CABLE ASSY	ASSEMBLY NO. 1207-00-0004 PAGE: 1	REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE CABLE ASSY IEC (GPIB) OPTION
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES ± 1° .XX ± .030		
	DO NOT SCALE DWG		
	SCALE	MODEL NO 159-005	DWG NO 1207-00-0004 REV
		CODE IDENT 23338	SHEET 1 OF 1

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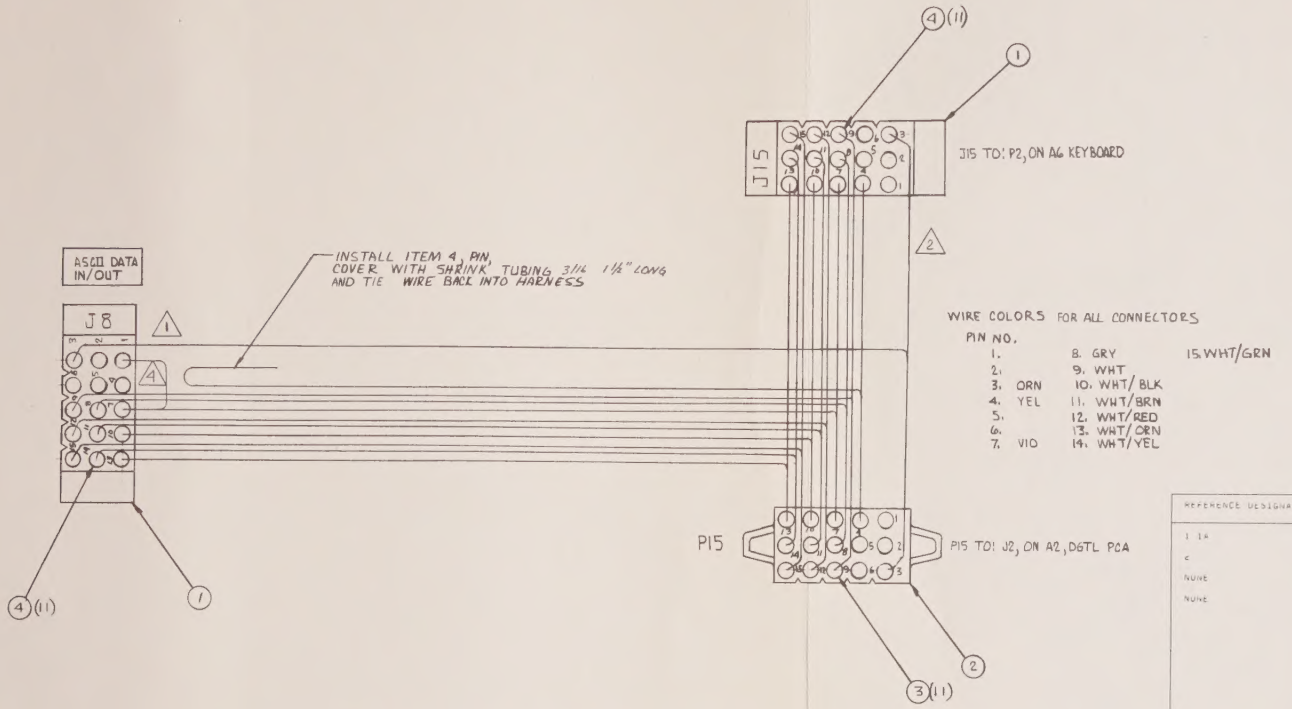
REV	ECN	BY	DATE	APP



WIRE COLORS FOR ALL CONNECTORS

PIN NO.			
1.		8. GRY	15. WHT/GRN
2.		9. WHT	
3.	ORN	10. WHT/BLK	
4.	YEL	11. WHT/BRN	
5.		12. WHT/RED	
6.		13. WHT/ORN	
7.	VIO	14. WHT/YEL	

REFERENCE DESIGNATORS	PART DESCRIPTION	OMIC-MFGR-PART NO.	MFGR	WAVETEK NO.	QTY/PC
1 1A	CONN,15PIN	03-04-1151	MOLEX	2100-02-0012	2
2	PLUG,15PIN	03-04-2151	MOLEX	2100-02-0013	1
NONE	PIN,MALE	02-04-2110	MOLEX	2100-03-0005	11
NONE	PIN,FEMALE	02-04-1110	MOLEX	2100-03-0002	22

WAVETEK PARTS LIST	TITLE CABLE ASSY	ASSEMBLY NO. 1203-00-0005 PAGE: 1	REV

△4 WIRE COLOR TO BE VIO CUT WIRE TO A LENGTH OF 1.00

3. TIE WIRES USING SMALL CABLE TYE 23M AS REQ.

△2 CUT WIRES TO A LENGTH OF 3.00

△1 CUT WIRES TO A LENGTH OF 16.50

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BARNETT	DATE 8/6/74	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	ENGINEER [signature]	9/10/74	TITLE CONNECTOR ASSY ASCII DATA IN/OUT
FINISH WAVETEK PROCESS	RELEASE APPROV [signature]	12/10/74	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 158/159	DWG NO. 1203-00-0003 REV
	SCALE NONE	CODE IDENT 23338	SHEET 2 OF 2

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